



ICCAD 2022 CONFERENCE PROGRAM

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Cadence Talk at ICCAD

Join us on Monday, October 31, from 6:00pm to 7:00pm in Saint Tropez, to hear a talk about "Cadence - Accelerating Innovation" by David Junkin, Academic Network Program Director.





Bridging academia and industry to create new opportunities for innovation and collaboration



Meet the Synopsys Academic & Research Alliances Team to learn more about our programs!

Office Hours:

Monday–Wednesday

10:00 a.m.–12:00 p.m and 4:15–5:45 p.m

Location: Foyer (Near Registration Desk)

Email us at SARA-NA@synopsys.com to schedule a time to sync up.



Scan the QR code for more information, or visit: [Synopsys.com/SARA](https://www.synopsys.com/SARA)

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General Information

Registration Hours & Location

Location: Foyer

Sunday, October 30	7:30am-5:00pm
Monday, October 31	7:00am-7:00pm
Tuesday, November 1	7:00am-7:00pm
Wednesday, November 2	7:00am-6:00pm
Thursday, November 3	7:00am-4:00pm

CONFlux

Access the virtual platform to build out your schedule, watch presentation videos, download slides, connect to the live virtual sessions and other attendees! Go to <https://iccad2022.conflux.events/welcome> and use the password emailed to you a few days before the event for access.

Posters

This year, all technical presenters are asked to bring a copy of their poster to be displayed during their oral session for further discussion after their talk. Poster boards will be available in each breakout room, and authors are asked to pin up their poster 15 minutes before their session starts.

Speaker's Breakfast

Location: Terrazza Ballroom

Please attend the day of your presentation!

Monday, October 31	7:30-8:30am
Tuesday, November 1	8:00-9:00am
Wednesday, November 2	8:00-9:00am

Parking

Attendees who will be driving in may park onsite, complimentary, for a day pass. Overnight parking is at a discounted, \$20/night.

ICCAD Social Media

Twitter: @ICCAD

LinkedIn: <https://www.linkedin.com/company/9289426>

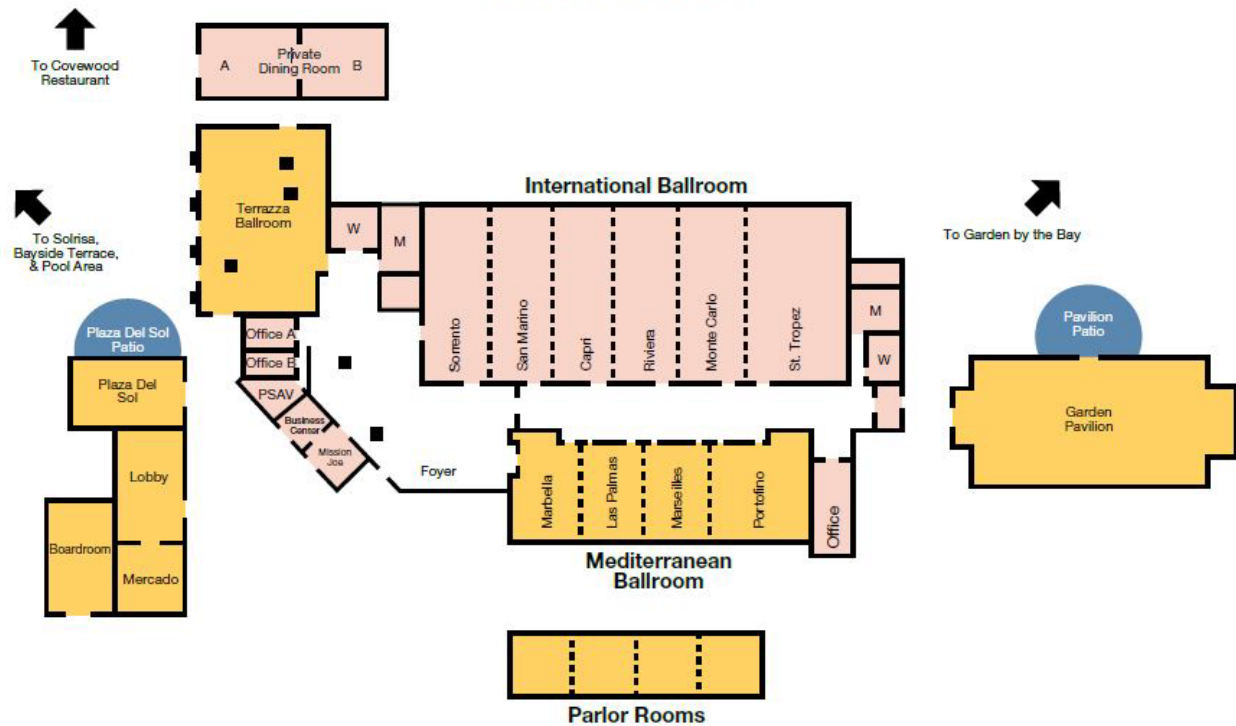
Conference Management



San Diego Mission Bay Resort

1775 E Mission Bay Dr.
San Diego, CA 92109

MEETING & BANQUET FACILITIES



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Welcome to ICCAD 2022

It is our pleasure to welcome you to the 41st edition of the International Conference on Computer-Aided Design!

Jointly sponsored by ACM and IEEE, ICCAD is the premier forum to explore new challenges, present leading-edge innovative solutions, and identify emerging technologies in the Electronic Design Automation (EDA) research areas. ICCAD covers the full range of Computer-Aided Design (CAD) topics – from device and circuit-level up through system-level, as well as post-CMOS design.

After two years of virtual conferences due to the global COVID-19 pandemic, we are excited to organize a hybrid conference from 30 October to 4 November 2022 in San Diego. The conference is primarily an in-person event enabling personal interactions and extensive networking, the aspects that cannot be replicated in virtual platforms. At the same time, we are offering virtual sessions for the speakers and the attendees who cannot attend in person due to travel restrictions or health issues. The virtual sessions are held fully online in the morning followed by the in-person sessions. Pre-recorded video presentations of all the talks, irrespective of whether they are part of a virtual or in-person session, are available on the virtual platform for all the attendees. The participants can discuss the papers with the authors through the virtual platform.

ICCAD has a long-standing tradition of producing cutting-edge, innovative technical program for attendees. Following the tradition, the members of the executive committee, the technical program committee, and numerous volunteers have spent an enormous effort to prepare an outstanding technical program for this year as well. We are glad to announce that we again had a significant increase in the number of regular paper submissions with a record 595 papers going through the complete peer-review process. This strong submission record amidst a global pandemic emphasizes the high relevance and the recognition of the conference within, but not limited to, the CAD community. For handling such an enormous submission number, we have carefully created 15 tracks and invited 203 outstanding technical program committee members from both industry and academia worldwide for these tracks. The TPC meeting was conducted again as an online event without compromising the quality of the double-blind review process. Finally, the program committee has selected 132 papers with an acceptance rate of 22% and yielded 43 regular sessions on diverse topics. Among the regular sessions, 28 will be held in-person while 15 sessions are virtual. In addition, we have ten special sessions and two embedded tutorials on topics that complement the regular sessions; almost all these sessions are in-person.

We are delighted to present three distinguished keynote speakers: the Monday morning keynote on Democratizing IC Design and Customized Computing will be given by Professor Jason Cong from the University of California, Los Angeles. On Tuesday, Professor Farinaz Koushanfar from the University of California San Diego will present the IEEE CEDA Luncheon Distinguished Lecture on Automated Cryptographically-Secure Private Computing. Shankar Krishnamoorthy from Synopsys will present the Wednesday keynote on Atoms to Silicon to Systems Hyper-Convergence to realize the next wave of semiconductor innovations. We hope you will find these keynotes inspiring, insightful and informative.

We have six interesting workshops on Thursday and one on Friday covering various new and established topics. Some of these workshops (Workshop on Accelerator Computer-Aided Design (ACCAD), Workshop on Hardware and Algorithms for Learning On-a-chip (HALO), Workshop on Open-Source EDA Technology (WOSET), and Top Picks in Hardware and Embedded Security) are long-time staples of ICCAD, while the Workshop on Zero Trust Hardware Architectures tests the waters for the first time. Two of these workshops are co-located with ICCAD: 24th ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP) and Sustainable Hardware Security (SUSHI). We hope that you will join the workshops that complement the ICCAD program.

Last but not the least, ICCAD hosts several contests and competitions. The CAD Contest is a challenging, multi-month, team-based research and development competition, focusing on advanced, real-world problems in the field of EDA. The CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of CAD and EDA. The ACM Student Research Competition (SRC) at ICCAD provides an opportunity for undergraduate and graduate students to share research results and exchange ideas with other students, judges, and conference attendees. This year, we are also debuting ACM/IEEE TinyML Design Contest --- a challenging, team-based, multi-month, research and development competition, focusing on real-world problems that require the implementation of machine learning algorithms on low-end microprocessors/microcontrollers. Finally, ICCAD 2022 is also featuring the first ACM SIGDA Job Fair.

Please let me emphasize again that ICCAD aims relentlessly at being the ultimate destination for cutting-edge EDA research and emerging CAD technologies. The organization of ICCAD is only possible with continuous support and help from the sponsors and many volunteers: the program chair with the program committee members, the organizers of the workshops, contests, and job fairs, and all members of the organization committee. We are grateful for their commitment and dedicated contributions to making ICCAD a successful conference. We appreciate your attendance, interaction, and support in shaping this year's hybrid event into a memorable one.

General Chair of ICCAD 2022
Tulika Mitra
National University of Singapore

Awards Committee

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee

Masanori Hashimoto (CHAIR) (Kyoto University)
Hussam Amrouch (University of Stuttgart)
Jianli Chen (Fudan University)
Tsung-wei Huang (University of Utah)
Zhuo Feng (Stevens Institute of Technology)
Richard Shi (University of Washington)
Farinaz Koushanfar (University of California, San Diego)
Alan Mishchenko (University of California, Berkeley)

William J. McCalla ICCAD Ten Year Retrospective Most Influential Paper Award Selection Committee

Ulf Schlichtmann (CHAIR) (The Technical University of Munich)
Jie Han (University of Alberta)
Iris Hui-Ru Jiang (National Taiwan University)
David Z. Pan (University of Texas at Austin)
Marilyn C. Wolf (University of Nebraska – Lincoln)

Awards

IEEE/ACM William J. McCalla ICCAD Best Paper Awards

Back-end:

Session 1D: SpecPart: A Supervised Spectral Framework for Hypergraph Partitioning Solution Improvement

Ismail Bustany (AMD)
Andrew Kahng (UCSD)
Ioannis Koutis (New Jersey Institute of Technology)
Bodhisatta Pramanik (Iowa State University)
Zhiang Wang (University of California San Diego)

Front-end:

Session 5D: Attack Directories on ARM big.LITTLE Processors

Zili Kou (Hong Kong University of Science and Technology)
Sharad Sinha (Indian Institute of Technology Goa)
Wenjian He (Hong Kong University of Science and Technology)
Wei Zhang (Hong Kong University of Science and Technology)

IEEE/ACM William J. McCalla ICCAD Best Paper Award Nominations

Front-end:

Session 8D: Logic Synthesis for Digital In-Memory Computing

Muhammad Rashedul Haq Rashed (University of Central Florida)
Sumit Kumar Jha (University of Texas at San Antonio)
Rickard Ewetz (University of Central Florida)

Session 7D: ObfuNAS: A Neural Architecture Search-based DNN Obfuscation Approach

Tong Zhou (Northeastern University)
Shaolei Ren (UC Riverside)
Xiaolin Xu (Northeastern University)

Back-end:

Session 11B: DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography

Qipan Wang (Peking University)
Xiaohan Gao (Peking University)
Yibo Lin (Peking University)
Runsheng Wang (Peking University)
Ru Huang (Peking University)

Session 7A: TransSizer: A Novel Transformer-Based Fast Gate Sizer

Siddhartha Nath (NVIDIA Corp)
Geraldo Pradipta (NVIDIA Corp)
Corey Hu (NVIDIA Corp)
Tian Yang (NVIDIA Corp)
Brucek Khailany (NVIDIA)
Haoxing Ren (NVIDIA Corporation)

Awards

William J. McCalla ICCAD Ten Year Retrospective Most Influential Paper Award

On reconfiguration-oriented approximate adder design and its application

Rong Ye (The Chinese University of Hong Kong)

Ting Wang (The Chinese University of Hong Kong)

Feng Yuan (The Chinese University of Hong Kong)

Rakesh Kumar (University of Illinois at Urbana-Champaign)

Qiang Xu (The Chinese University of Hong Kong)

In 2013 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 48-54. IEEE, 2013.

The award is given to the paper judged to be the most influential on research and industry practice in computer-aided design of integrated circuits over the ten years since its original appearance at ICCAD. The awards are jointly sponsored by IEEE Council on Electronic Design Automation (IEEE CEDA) and the ACM Special Interest Group on Design Automation (ACM SIGDA).

2022 IEEE CEDA Ernest S. Kuh Early Career Award

Bei Yu (The Chinese University of Hong Kong)

For contributions to machine learning in physical design and Design for Manufacturability

2022 IEEE CEDA Outstanding Service Recognition

Rolf Drechsler (University of Bremen)

For outstanding service to the EDA community as ICCAD General Chair in 2021

Keynote Speaker – Jason Cong



Jason Cong

UCLA Computer Science Department

Director, Center for Domain-Specific Computing (CDSC)

Jason Cong is the Volgenau Chair for Engineering Excellence Professor (and former Department Chair) at the UCLA Computer Science Department, with joint appointment from the Electrical Engineering Department, the director of Center for Domain-Specific Computing (CDSC), and the director of VLSI Architecture, Synthesis, and Technology (VAST) Laboratory. Dr. Cong's research interests include electronic design automation, novel architectures and compilation for customizable computing, and quantum computing. He has close to 500 publications in these areas, including 16 best paper awards, three 10-Year Most Influential Paper Awards, and three papers inducted to the FPGA and Reconfigurable Computing Hall of

Fame. He and his former students co-founded AutoESL and Falcon Computing Solutions. Both were acquired by Xilinx and led to the most widely used high-level synthesis tool for FPGAs. He was elected to an IEEE Fellow in 2000, ACM Fellow in 2008, and the National Academy of Engineering in 2017. He is the recipient of the 2022 IEEE Robert Noyce Medal for fundamental contributions to electronic design automation and FPGA design methods.

Democratizing IC Design and Customized Computing

The electronic design automation (EDA) traditionally serves the hardware design community. As we enter the era of customized computing with increasing amount of computation moves from general-purpose CPUs to domain-specific accelerators (DSAs) due to their performance and energy efficiency, there is a pressing need and opportunity for the EDA community to empower millions of software programmers to create their own DSAs to accelerate the compute-intensive portion of their applications. High-level synthesis (HLS) made an important progress in this direction, but far from sufficient. In this talk, I shall discuss the recent progresses in this area, including microarchitecture guided optimization, such as automated systolic array generation, automated source-to-source transformation based on graph-based neural networks and meta learning, and support of domain-specific languages widely used in the software community. I hope to see the ICCAD community in joining the effort of broadening the participation of IC designs and customized computing.

CEDA Keynote Speaker - Farinaz Koushanfar



Farinaz Koushanfar

Henry Booker Scholar Professor of ECE at the University of California San Diego (UCSD)

Farinaz Koushanfar is the Henry Booker Scholar Professor of ECE at the University of California San Diego (UCSD), where she is also the founding co-director of the UCSD Center for Machine-Intelligence, Computing & Security (MICS). Her research addresses several aspects of secure and efficient computing, with a focus on hardware and system security, robust machine learning under resource constraints, intellectual property (IP) protection, as well as practical privacy-preserving computing. Dr. Koushanfar is a fellow of the Kavli Frontiers of the National Academy of Sciences and a fellow of IEEE. She has received a number of awards and honors including the Presidential Early Career Award for Scientists and Engineers (PECASE) from President Obama, the ACM SIGDA Outstanding New Faculty Award, Cisco

IoT Security Grand Challenge Award, MIT Technology Review TR-35, Qualcomm Innovation Awards, Intel Collaborative Awards, Young Faculty/CAREER Awards from NSF, DARPA, ONR and ARO, as well as several best paper awards.

Automated Cryptographically-Secure Private Computing: From Logic and Mixed-Protocol Optimization to Centralized and Federated ML Customization

Over the last four decades, much research effort has been dedicated to designing cryptographically-secure methods for computing on encrypted data. However, despite the great progress in research, adoption of the sophisticated crypto methodologies has been rather slow and limited in practical settings. Presently used heuristic and trusted third party solutions fall short in guaranteeing the privacy requirements for the contemporary massive datasets, complex AI algorithms, and the emerging collaborative/distributed computing scenarios such as blockchains.

In this talk, we outline the challenges in the state-of-the-art protocols for computing on encrypted data with an emphasis on the emerging centralized, federated, and distributed learning scenarios. We discuss how in recent years, giant strides have been made in this field by leveraging optimization and design automation methods including logic synthesis, protocol selection, and automated co-design/co-optimization of cryptographic protocols, learning algorithm, software, and hardware. Proof of concept would be demonstrated in the design of COINN, the present state-of-the-art framework for cryptographically-secure deep learning on encrypted data. We conclude by discussing the practical challenges in the emerging private robust learning and distributed/ federated computing scenarios as well as the opportunities ahead.

Keynote Speaker - Shankar Krishnamoorthy



Shankar Krishnamoorthy

General Manager, EDA Group, Synopsys

Shankar Krishnamoorthy is the General Manager of the EDA Group, leading the team behind the design and verification software platforms from Synopsys. His group innovates across a broad spectrum of EDA technologies including simulation, static analysis, debug, synthesis, signoff analysis, place-and-route, test automation, and formal verification solutions. Prior to this role, he was General Manager of the Digital Design Group, with responsibility for the Synopsys digital design platform. In earlier roles, he served as Senior Vice President of the Digital Implementation Group, delivering several game-changing innovations including Fusion Compiler™, RTL Architect, 3DIC Compiler, and TestMAX solutions. Before rejoining Synopsys in 2017, Shankar was at Mentor Graphics, where he

served as General Manager of the IC Design Solutions Division. He joined Mentor in 2007 with the acquisition of Sierra Design Automation, where he was Founder and CTO. Prior to Sierra Design, Shankar led Synopsys' physical synthesis and logic synthesis R&D organizations. Shankar received his M.S. in Computer Science from the University of Texas, Austin, and his bachelor's degree in Computer Science from the Indian Institute of Technology, Bombay.

Atoms To Silicon to Systems Hyper-Convergence: The Way Forward in the Angstrom Era

AI, fueled by semiconductor compute power, is driving the growing intelligence in the 'smart everything' world we live in. Silicon is at the heart of the new wave of products enabling this intelligence. At the same time, chips' scaling, performance, energy efficiency and cost are being challenged like never before.

In this keynote, Shankar Krishnamoorthy, general manager of the EDA Group at Synopsys, shares his views on why it is imperative for the semiconductor industry to take a holistic atom to silicon to systems approach to address these challenges and what solutions are needed to realize the next wave of semiconductor innovations.

CADathlon: Sunday, October 30

CADathlon 2022 will be held in the hybrid format, you will be competing against the bests around the world.

The **CADathlon** is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork. As the “**Olympic games of EDA**,” the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field.

The contest is open to **two-person teams** of **undergraduate**/graduate students specializing in CAD and currently full-time enrolled in a Ph.D. granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Partial or full travel grants are provided to qualifying students. CADathlon competition consists of *six* problems in the following areas:

- Circuit Design & Analysis
- Physical Design & Design for Manufacturability
- Logic & High-Level Synthesis
- System Design & Analysis
- Functional Verification & Testing
- Future technologies (Bio-EDA, Security, AI, etc.)

More specific information about the problems and relevant research papers will be released on the Internet **one week prior** to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges’ test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given.

The team that earns the highest score is declared the winner. In addition to handsome trophies, the first place and the second-place teams receive cash award, and the contest winners will be announced at the ICCAD conference.

Organization Committee:

Chair: Pei-Yu Billy Lee (*MediaTek, Taiwan*)
Co-chair: Yu-Guang Chen (*National Central University, Taiwan*)
Co-chair: Jeff (Jun) Zhang (*Arizona State University*)

Day-at-a-Glance: Monday, October 31

PDT	St. Tropez	Monte Carlo	Riviera	Capri
7:30-8:30am	Terazza Ballroom Speaker Breakfast			
8:30-10:00am	Monte Carlo & St. Tropez Combined Opening & Keynote Democratizing IC Design and Customized Computing <i>Jason Cong, UCLA & CDSC</i>			
10:00-10:30am	Foyer Coffee Break			
10:30am-12:30pm	1A – Special Session: The Role of Graph Neural Networks in Electronic Design Automation	1B – Compiler and System-level Techniques for Efficient Machine Learning	1C – Special Session: Addressing Sensor Security through Hardware/Software Co-design	1D – Advances in Partitioning and Physical Optimization
11:00am-1:00pm				Private Dining Room SRC Poster
12:30-1:30pm	Bayside Terrace (Pavilion if raining) Lunch			
1:45 -3:45pm	2A – Special Session: Democratizing Design Automation with Open-Source tools: perspectives, opportunities, and challenges	2B – Accelerators on A New Horizon	2C – Special Session: CAD for Confidentiality of Hardware IPS	2D – Analyzing Reliability, Defects and Patterning
3:45-4:15pm	Foyer Coffee Break			
4:15-5:45pm	3A – New Frontier in Verification Technology	3B – Lower Power Edge Intelligence	3C – Crossbars, Analog Accelerators for Neural Networks and Neuromorphic Computing based on Printed Electronics	3D – Designing DNN Accelerators
6:00-7:00pm	Cadence –Accelerating Innovation	6:00-7:30 SRC Oral		

Special Session

Keynote

Social

Industry Sponsor Session

Competition

Day-at-a-Glance: Tuesday, November 1

PDT	Virtual Sessions			
6:00-7:00am	4A – Novel Chiplet Approaches from Interconnect to System	4B – Architecture for DNN Acceleration	4C – Multi-Purpose Fundamental Digital Design Improvements	4D – GPU Accelerated Routing Algorithms
7:10-8:30am	5A – Breakthroughs in Synthesis – Infrastructure and ML Assist I	5B – Smart Search	5C – Reconfigurable Computing: Accelerators and Methodologies I	5D – Hardware Security: Attacks and Countermeasures
In-Person Sessions				
PDT	St. Tropez	Monte Carlo	Riviera	Capri
8:00-9:00am	Terazza Ballroom Speaker Breakfast			
9:00-10:30am	6A – Advanced VLSI Routing and Layout Learning	6B – Physical Attacks and Countermeasures	6C – Tutorial: Polynomial Formal Verification: Ensuring Correctness under Resource Constraints	6D – Scalable Verification Technologies
10:30-11:00am	Foyer Coffee Break			
11:00am-12:30pm	7A – Optimizing Digital Design Aspects: From Gate Sizing to Multi-Bit Flip-Flops	7B – Energy Efficient Hardware Acceleration and Stochastic Computing	7C – Special Session: Approximate Computing and the Efficient Machine Learning Expedition	7D – Co-search Methods and Tools
12:30-2:00pm	Pavilion CEDA Keynote Lunch (first come, first served) Automated Cryptographically-Secure Private Computing: From Logic and Mixed-Protocol Optimization to Centralized and Federated ML Customization <i>Farinaz Koushanfar, UCSD</i>			
2:00-3:00pm	8A – Reconfigurable Computing: Accelerators and Methodologies II	8B – Compute-in-Memory for Neural Networks	8C – Breakthroughs in Synthesis – Infrastructure and ML Assist II	8D – In-Memory Computing Revisited
3:00-3:30pm	Foyer Coffee Break			
3:30-5:30pm	9A – Special Session: 2022 CAD contest at ICCAD	9B – Architectures and Methodologies for Advanced Hardware Security	9C – Special Session: The Dawn of Domain-specific Hardware Accelerators for Robotic Computing	9D – From Logical to Physical Qubits: New Models and Techniques for Mapping
6:00-9:00pm	Pavilion Job Fair & SIGDA Dinner (first come, first served)			

Tutorial

Special Session

Keynote

Social

Day-at-a-Glance: Wednesday, November 2

PDT	Virtual Sessions				
6:00-7:00am	10A – Smart Embedded Systems	10B – Analog/Mixed-Signal Simulation, Layout and Packaging	10C – Advanced PIM and Biochip Technology and Stochastic Computing	10D – On Automating Heterogeneous Designs	Virtual Job Fair
7:10-8:30am	11A – Special Session: Quantum Computing to Solve Chemistry, Physics and Security Problems	11B – Make Patterning Work	11C – Advanced Verification Technologies	11D – Routing with Cell Movement	
In-Person Sessions					
PDT	St. Tropez	Monte Carlo	Riviera	Capri	
8:00-9:00am	Terazza Ballroom Speaker Breakfast				
9:00-10:00am	Monte Carlo & St. Tropez Combined Opening & Keynote Atoms to Silicon to Systems Hyper-Convergence: The Way Forward in the Angstrom Era <i>Shankar Krishnamoorthy, Synopsys</i>				
10:00-10:30am	Foyer Coffee Break				
10:30am-12:30pm	12A – Special Session: Hardware Security Through Reconfigurability: Attacks, Defenses, and Challenges	12B – Performance, Power and Temperature Aspects in Deep Learning	12C – Tutorial: TorchQuantum: A Fast Library for Parameterized Quantum Circuits	12D – Emerging Machine Learning Primitives: from Technology to Application	
12:30-1:30pm	Bayside Terrace (Pavilion if raining) Lunch				
1:45-3:15pm	13A – Design for Low Energy, Low Resources but High Quality	13B – Microarchitectural Attacks and Countermeasures	13C – Genetic Circuits meet Ising Machines	TinyML Competition	
3:15-3:45pm	Foyer Coffee Break				
3:45-5:45pm	14A – Energy Efficient Neural Networks via Approximate Computation	14B – Algorithms and Tools for Security Analysis and Secure Hardware Design	14C – Special Session: Making ML reliable: From devices to systems to software	14D – Autonomous Systems and Machine Learning on Embedded Systems	

Special Session

Competition

Tutorial

Keynote

Social

Technical Program: Monday, October 31

10:30 AM – 12:30 PM, St. Tropez

1A Special Session: The Role of Graph Neural Networks in Electronic Design Automation

Session Chair: Jeyavijayan Rajendran (Texas A&M)

Why Should You Use Graph Neural Network for VLSI Design Automation?

Haoxing Ren (NVIDIA Corporation)

Sid Nath (NVIDIA Corporation)

Yan Zhang (NVIDIA Corporation)

Hao Chen (University of Texas at Austin)

Mingjie Liu (University of Texas at Austin)

On Advancing Physical Design using Graph Neural Networks

Yi-Chen Lu (Georgia Institute of Technology)

Sung Kyu Lim (Georgia Institute of Technology)

Applying GNNs to Timing Estimation at RTL

Daniela Sánchez Lopera (Infineon Technologies AG, Germany and Technical University of Munich, Germany)

Wolfgang Ecker (Infineon Technologies AG, Germany and Technical University of Munich, Germany)

Embracing Graph Neural Networks for Hardware Security

Lilas Alrahis (New York University Abu Dhabi)

Satwik Patnaik (Texas A&M University)

Muhammad Shafique (New York University Abu Dhabi)

Ozgur Sinanoglu (New York University Abu Dhabi)

Graph Neural Network Techniques for Digital and Analog Design Predictions

Jiang Hu (Texas A&M University)

Technical Program: Monday, October 31

10:30 AM – 12:30 PM, Monte Carlo

1B Compiler and System-level Techniques for Efficient Machine Learning

Session Chair: Sri Parameswaran (UNSW)

Session Co-Chair: Martin Rapp (KIT)

Fine-Granular Computation and Data Layout Reorganization for Improving Locality

Mahmut Kandemir (PSU)

Xulong Tang (University of Pittsburgh)

Jagadish Kotra (AMD Research)

Mustafa Karakoy (TUBITAK-BILGEM)

An MLIR-based Compiler Flow for System-Level Design and Hardware Acceleration

Nicolas Bohm Agostini (Northeastern University)

Serena Curzel (Politecnico di Milano)

Vinay Amatya (Pacific Northwest National Laboratory)

Cheng Tan (Microsoft)

Marco Minutoli (Pacific Northwest National Laboratory)

Vito Giovanni Castellana (Pacific Northwest National Laboratory)

Joseph Manzano (Pacific Northwest National Laboratory)

David Kaeli (Northeastern University)

Antonino Tumeo (Pacific Northwest National Laboratory)

Physics-aware Differentiable Discrete Codesign for Diffractive Optical Neural Networks

Yingjie Li (University of Utah)

Ruiyang Chen (University of Utah)

Weilu Gao (University of Utah)

Cunxi Yu (University of Utah)

Big-Little Chiplets for In-Memory Acceleration of DNNs: A Scalable Heterogeneous Architecture

Gokul Krishnan (Arizona State University)

A. Alper Goksoy (University of Wisconsin – Madison)

Sumit Mandal (University of Wisconsin-Madison)

Zhenyu Wang (Arizona State University)

Chaitali Chakrabarti (Arizona State University)

Jae-sun Seo (Arizona State University)

Umit Ogras (University of Wisconsin – Madison)

Yu Cao (Arizona State University)

Technical Program: Monday, October 31

10:30 AM – 12:30 PM, Riviera

1C Special Session: Addressing Sensor Security through Hardware/Software Co-design

Session Chair: Marilyn Wolf (University of Nebraska)

Attacks on Image Sensors

Marilyn Wolf (University of Nebraska — Lincoln)

Kruttdipta Samal (University of Nebraska — Lincoln)

False Data Injection Attacks on Sensor Systems

Dimitrios Serpanos (Computer Technology Institute and University of Patras)

Stochastic Mixed-Signal Circuit Design for In-sensor Privacy

Ningyuan Cao (University of Notre Dame)

Jianbo Liu (University of Notre Dame)

Boyang Cheng (University of Notre Dame)

Muya Chang (University of Notre Dame)

Sensor Security: Current Progress, Research Challenges, and Future Roadmap

Anomadarshi Barua (University of California, Irvine)

Mohammad Abdullah Al Faruque (University of California, Irvine)

Technical Program: Monday, October 31

10:30 AM – 12:30 PM, Capri

1D Advances in Partitioning and Physical Optimization

Session Chair: Markus Olbrich (Leibniz Universität Hannover)

Session Co-Chair: Yu-Guang Chen (National Central University)

SpecPart: A Supervised Spectral Framework for Hypergraph Partitioning Solution Improvement **Best**

Paper Award Nomination

Ismail Bustany (AMD)

Andrew Kahng (UCSD)

Ioannis Koutis (New Jersey Institute of Technology)

Bodhisatta Pramanik (Iowa State University)

Zhiang Wang (University of California San Diego)

HyperEF: Spectral Hypergraph Coarsening by Effective-Resistance Clustering

Ali Aghdaei (Stevens Institute of Technology)

Zhuo Feng (Stevens Institute of Technology)

Design and Technology Co-optimization Utilizing Multi-bit Flip-flop Cells

Soomin Kim (Seoul National University)

Taewhan Kim (Seoul National University)

Transitive Closure Graph-Based Warpage-aware Floorplanning for Package Designs

Yang Hsu (National Taiwan University)

Min-Hsuan Chung (National Taiwan University)

Yao-Wen Chang (National Taiwan University)

Ci-Hong Lin (CoreTech System Co., Ltd.)

Technical Program: Monday, October 31

1:45 PM – 3:45 PM, St. Tropez

2A Special Session: Democratizing Design Automation with Open-Source tools: perspectives, opportunities, and challenges

Session Chair: Antonino Tumeo (Pacific Northwest National Laboratory)

A Mixed Open-Source and Proprietary EDA Commons for Education and Prototyping

Andrew Kahng (UCSD)

SODA Synthesizer: An Open-source, Multi-level, Modular, Extensible compiler from High-level Frameworks to Silicon

Nicolas Bohm Agostini (PNNL & Northeastern University)

Ankur Limaye (Pacific Northwest National Laboratory)

Serena Curzel (PNNL & Politecnico di Milano)

Marco Minutoli (Pacific Northwest National Laboratory)

Vito Giovanni Castellana (Pacific Northwest National Laboratory)

Joseph Manzano (Pacific Northwest National Laboratory)

Fabrizio Ferrandi (Politecnico di Milano)

Antonino Tumeo (Pacific Northwest National Laboratory)

OpenFPGA & LSOracle: Open-source FPGA Synthesis Guided by Machine Learning

Scott Temple (University of Utah)

Ashton Snelgrove (University of Utah)

Grant Brown (University of Utah)

Pierre-Emmanuel Gaillardon (University of Utah)

A Scalable Methodology for Agile Chip Development with Open-Source Hardware Components

Maico Cassel dos Santos (Columbia University)

Tianyu Jia (Harvard University)

Martin Cochet (IBM Research)

Karthik Swaminathan (IBM Research)

Joseph Zuckerman (Columbia University)

Paolo Mantovani (Columbia University)

Davide Giri (Columbia University)

Jeff Jun Zhang (Harvard University)

Erik Jens Loscalzo (Columbia University)

Gabriele Tombesi (Columbia University)

Kevin Tien (IBM Research)

Nandhini Chandramoorthy (IBM Research)

John-David Wellman (IBM Research)

David Brooks (Harvard University)

Gu-Yeon Wei (Harvard University)

Kenneth Shepard (Columbia University)

Luca P. Carloni (Columbia University)

Pradip Bose (IBM Research)

Technical Program: Monday, October 31

1:45 PM – 3:45 PM, Monte Carlo

2B Accelerators on A New Horizon

Session Chair: Vaibhav Verma (Qualcomm)

Session Co-Chair: Georgios Zervakis (KIT)

GraphRC: Accelerating Graph Processing on Dual-addressing Memory with Vertex Merging

Wei Cheng (National Cheng Kung University)

Chun-Feng Wu (Harvard University)

Yuan-Hao Chang (Academia Sinica)

Ing-Chao Lin (National Cheng Kung University)

Spatz: A Compact Vector Processing Unit for High-Performance and Energy-Efficient Shared-L1 Clusters

Matheus Cavalcante (ETH Zurich)

Domenic Wuethrich (ETH Zürich)

Matteo Perotti (ETH Zürich)

Samuel Riedel (ETH Zurich)

Luca Benini (Universite di Bologna and ETH Zurich)

Qilin: Enabling Performance Analysis and Optimization of Shared-Virtual Memory Systems with FPGA Accelerators

Edward Richter (University of Illinois at Urbana-Champaign)

Deming Chen (UIUC)

ReSiPI: A Reconfigurable Silicon-Photonic 2.5D Chiplet Network with PCMs for Energy-Efficient Interposer Communication

Ebadollah Taheri (Colorado State University)

Sudeep Pasricha (Colorado State University)

Mahdi Nikdast (Colorado State University)

1:45 PM – 3:45 PM, Riviera

2C Special Session: CAD for Confidentiality of Hardware IPS

Session Chair: Swarup Bhunia (University of Florida)

Hardware IP Protection against Confidentiality Attacks and Evolving Role of CAD Tool

Swarup Bhunia (University of Florida)

Amitabh Das (AMD)

Saverio Fazzari (Booz Allen Hamilton)

Vivian Kammler (Sandia National Laboratories)

David Kehlet (Intel)

Jeyavijayan Rajendran (Texas A&M University)

Ankur Srivastava (University of Maryland)

Technical Program: Monday, October 31

1:45 PM – 3:45 PM, Capri

2D Analyzing Reliability, Defects and Patterning

Session Chair: Gaurav Rajavendra Reddy (Intel)

Session Co-Chair: Kostas Adam (Siemens EDA)

Pin Accessibility and Routing Congestion Aware DRC Hotspot Prediction using Graph Neural Network and U-Net

Kyeonghyeon Baek (Seoul National University)

Hyunbum Park (Seoul National University)

Suwan Kim (Seoul National University)

Kyu-Myung Choi (Seoul National University)

Taewhan Kim (Seoul National University)

A Novel Semi-Analytical Approach for Fast Electromigration Stress Analysis in Multi-Segment Interconnects

Olympia Axelou (University of Thessaly)

Nestor Evmorfopoulos (University of Thessaly)

George Floros (University of Thessaly)

Georgios Stamoulis (University of Thessaly)

Sachin S. Sapatnekar (University of Minnesota)

HierPINN-EM: Fast Learning-Based Electromigration Analysis for Multi-Segment Interconnects Using Hierarchical Physics-informed Neural Network

Wentian Jin (University of California, Riverside)

Liang Chen (University of California, Riverside)

Subed Lamichhane (University of California, Riverside)

Mohammad Amir Kavousi (University of California, Riverside)

Sheldon Tan (University of California at Riverside)

Sub-resolution Assist Feature Generation with Reinforcement Learning and Transfer Learning

Guan Ting Liu (National Taiwan University)

Wei-Chen Tai (National Taiwan University)

Yi-Ting Lin (National Taiwan University)

Iris Hui-Ru Jiang (National Taiwan University)

James Shiely (Synopsys)

Pu-Jen Cheng (National Taiwan University)

Technical Program: Monday, October 31

4:15 PM – 5:45 PM, St. Tropez

3A New Frontier in Verification Technology

Session Chair: Jyotirmoy Vinay Deshmukh (University of South California)

Session Co-Chair: Zahra Ghodsi (University of California, San Diego)

Automatic Test Configuration and Pattern Generation (ATCPG) for Neuromorphic Chips

I-Wei Chiu (National Taiwan University)

Xin-Ping Chen (National Taiwan University)

Jennifer Hu (Ming Chuan University)

James Chien-Mo Li (National Taiwan University)

ScaleHD: Robust Brain-Inspired Hyperdimensional Computing via Adaptive Scaling

Sizhe Zhang (Villanova University)

Mohsen Imani (University of California Irvine)

Xun Jiao (Villanova University)

Quantitative Verification and Design Space Exploration Under Uncertainty with Parametric Stochastic Contracts

Chanwook Oh (University of Southern California)

Michele Lora (University of Southern California)

Pierluigi Nuzzo (University of Southern California)

4:15 PM – 5:45 PM, Monte Carlo

3B Low Power Edge Intelligence

Session Chair: Sabya Das (Synopsys)

Session Co-Chair: Jiang Hu (TAMU)

Reliable Machine Learning for Wearable Activity Monitoring: Novel Algorithms and Theoretical Guarantees

Dina Hussein (Washington State University)

Taha Belkhouja (Washington State University)

Ganapati Bhat (Washington State University)

Jana Doppa (Washington State University)

Neurally-Inspired Hyperdimensional Classification for Efficient and Robust Biosignal Processing

Yang Ni (University of California, Irvine)

Nicholas Lesica (University College London)

Fan-Gang Zeng (University of California, Irvine)

Mohsen Imani (University of California Irvine)

EVE: Environmental Adaptive Neural Network Models for Low-power Energy Harvesting System

Sahidul Islam (The University of Texas at San Antonio)

Shanglin Zhou (University of Connecticut)

Ran Ran (Lehigh University)

Yufang Jin (UTSA)

Wujie Wen (Lehigh University)

Caiwen Ding (University of Connecticut)

Mimi Xie (The University of Texas at San Antonio)

Technical Program: Monday, October 31

4:15 PM – 5:45 PM, Riviera

3C Crossbars, Analog Accelerators for Neural Networks, and Neuromorphic Computing based on Printed Electronics

Session Chair: Hussam Amrouch (University of Stuttgart)

Session Co-Chair: Sheldon Tan (UCI)

Designing Energy-Efficient Decision Tree Memristor Crossbar Circuits using Binary Classification Graphs

Pranav Sinha (Oakland University)

Sunny Raj (Oakland University)

Fuse and Mix: MACAM-Enabled Analog Activation for Energy-Efficient Neural Acceleration

Hanqing Zhu (University of Texas at Austin)

Keren Zhu (University of Texas at Austin)

Jiaqi Gu (The University of Texas at Austin)

Harrison Jin (The University of Texas at Austin)

Ray Chen (The University of Texas at Austin)

Jean Anne Incorvia (The University of Texas at Austin)

David Z. Pan (University of Texas at Austin)

Aging-Aware Training for Printed Neuromorphic Circuits

Haibin Zhao (Karlsruhe Institute of Technology)

Michael Hefenbrock (Karlsruhe Institute of Technology)

Michael Beigl (Karlsruhe Institute of Technology)

Mehdi Tahoori (Karlsruhe Institute of Technology)

4:15 PM – 5:45 PM, Capri

3D Designing DNN Accelerators

Session Chair: Elliott Delaye (AMD)

Session Co-Chair: Yiyu Shi (U of Notre Dame)

Workload-Balanced Graph Attention Network Accelerator with Top-K Aggregation Candidates

Naebeom Park (Pohang University of Science and Technology)

Daehyun Ahn (Pohang University of Science and Technology)

Jae-Joon Kim (Seoul National University)

Re2fresh: A Framework for Mitigating Read Disturbance in ReRAM-based DNN Accelerators

Hyein Shin (KAIST)

Myeonggu Kang (Korea Advanced Institute of Science and Technology)

Lee-Sup Kim (KAIST)

FastStamp: Accelerating Neural Steganography and Digital Watermarking of Images on FPGAs

Shehzeen Hussain (UC San Diego)

Nojan Sheybani (UC San Diego)

Paarth Neekhara (UCSD)

Xinqiao Zhang (University of California San Diego)

Javier Duarte (UC San Diego)

Farinaz Koushanfar (University of California San Diego)

Cadence – Accelerating Innovation

Industry Sponsored Session



David Junkin

Academic Network Program Director

Dr. David Junkin has spent 25 years teaching engineers to design, implement, utilize, and sell integrated circuit chips. David has a passion for solving challenging, technical problems and collaboratively finding solutions with others—a passion that has driven his journey from a PhD in Physics to FAE management, from timing closure bootcamps to a signature technical NCG program at Texas Instruments. He is currently supporting Universities to foster the next generation of innovators as a Program Director for the Cadence Academic Network.

Cadence – Accelerating Innovation

Cadence is accelerating innovation by providing the tools and training needed for students to actively contribute to the Semiconductor industry. In line with the CHIPS Act, we have been supporting faculty, students, and design teams to develop the future workforce and cultivate the next generation of innovators. We're enabling engineers to design intelligent systems with Cadence tools – from hydrofoils for boats to automobiles like the McLaren F1.

Synopsys Academic & Research Alliances (SARA)

Through innovative collaborations, shared programs, and access to advanced technologies, Synopsys Academic & Research Alliances (SARA) is dedicated to furthering university research and education in the semiconductor industry. We aim to nurture the skills and provide the latest technology that is needed to bring the next generation of engineers into the workforce and research labs, and now enable researchers to share best practices and help build an academic community.

We are proud to announce Chief Security Officer Deirdre Hanford, has been appointed to the U.S. Department of Commerce's Industrial Advisory Committee, joining 24 distinguished members, as an advisory body that will provide guidance on a range of issues related to semiconductor research and development in support of CHIPS for America.

Meet the SARA team at ICCAD to find out more!

ICCAD Highlights

Meet SARA!

Please stop by our office hours during ICCAD and learn more about what the SARA team doing, and how to empower your education and research with Synopsys technology. Office Hours from Monday – Wednesday 10 a.m. to Noon and 4:15-5:45 p.m. in the foyer.



Harish Balan, North American University Program Manager and Global Ambassador

Harish Balan is celebrating his 18th year at Synopsys and has recently assumed the role of Global Ambassador of the Synopsys Academic & Research Alliances (SARA) Program. In this role, Harish builds on his extensive experience in applications engineering, product marketing and executive management, to expand on Synopsys' partnerships with universities and research institutions to help students, educators and researchers worldwide advance the state of the art and promote careers in electronic design. He is passionate about customer success, mentoring and coaching early career engineers and advocating for the EDA and semiconductor industry. Harish holds a master's degree in electrical engineering from the University of Texas at Austin and Executive Management credentials from Yale School of Management and Columbia University.

Can't make it? Set aside some time to meet by emailing, SARA-NA@synopsys.com

To learn more about SARA visit: [Synopsys.com/SARA](https://www.synopsys.com/SARA) and [subscribe to our newsletter](#).

The ACM Student Research Competition is an internationally recognized venue enabling undergraduate and graduate students who are ACM members to:

1. Experience the research world — for many undergraduates, this is a first!
2. Share research results and exchange ideas with other students, judges, and conference attendees.
3. Rub shoulders with academic and industry luminaries.
4. Understand the practical applications of their research.
5. Perfect their communication skills.
6. Receive prizes and gain recognition from ACM and the greater computing community.

The ACM Special Interest Group on Design Automation (ACM SIGDA) is organizing such an event in conjunction with the International Conference on Computer-Aided Design (ICCAD). Authors of accepted submissions will receive a grant from ACM SIGDA to attend the event at ICCAD. The event consists of several rounds, as described at <http://src.acm.org/> and <http://www.acm.org/student-research-competition>, where you can find more details on student eligibility and timeline. The first-place winner in the graduate category at SRC@ICCAD'20, Jiaqi Gu (the University of Texas at Austin), also won First Place in the 2021 ACM SRC Grand Finals!

Co-Chairs:

Callie (Cong) Hao (Georgia Institute of Technology)
Debjit Pal (The University of Illinois at Chicago)

Technical Program: Tuesday, November 1

6:00 AM – 7:00 AM, Virtual

4A Novel Chiplet Approaches from Interconnect to System (Virtual)

Session Chair: Xinfei Guo (SJTU)

GIA: A Reusable General Interposer Architecture for Agile Chiplet Integration

Fuping Li (Chinese Academy of Sciences)

Ying Wang (Chinese Academy of Sciences)

Yuanqing Cheng (Beihang University)

Yujie Wang (Chinese Academy of Sciences)

Yinhe Han (Chinese Academy of Sciences)

Huawei Li (Chinese Academy of Sciences)

Xiaowei Li (Chinese Academy of Sciences)

Accelerating Cache Coherence in Manycore Processor through Silicon Photonic Chiplet

Chengeng Li (The Hong Kong University of Science and Technology)

Fan Jiang (The Hong Kong University of Science and Technology)

Shixi Chen (The Hong Kong University of Science and Technology)

Jiaxu Zhang (The Hong Kong University of Science and Technology)

Yinyi LIU (The Hong Kong University of Science and Technology)

Yuxiang Fu (The Hong Kong University of Science and Technology)

Jiang Xu (The Hong Kong University of Science and Technology)

Re-LSM: A ReRAM-based Processing-in-Memory Framework for LSM-based Key-Value Store

Qian Wei (Shandong University)

Zhaoyan Shen (Shandong University)

Yiheng Tong (Shandong University)

Zhiping Jia (Shandong University)

Lei Ju (Shandong University)

Jiezhi Chen (Shandong University)

Bingzhe Li (Oklahoma State University)

Technical Program: Tuesday, November 1

6:00 AM – 7:00 AM, Virtual
4B Architecture for DNN Acceleration (Virtual)
Session Chair: Zhezhi He (SJTU)

Hidden-ROM: A Compute-in-ROM Architecture to Deploy Large-Scale Neural Networks on Chip with Flexible and Scalable Post-Fabrication Task Transfer Capability

Yiming Chen (Tsinghua University)
Guodong Yin (Tsinghua University)
Mingyen Lee (Tsinghua University)
Wenjun Tang (Tsinghua University)
Zekun Yang (Tsinghua University)
Yongpan Liu (Tsinghua University)
Huazhong Yang (Tsinghua University)
Xueqing Li (Tsinghua University)

DCIM-GCN: Digital Computing-in-Memory to Efficiently Accelerate Graph Convolutional Networks

Yikan Qiu (Peking University)
Yufei Ma (Peking University)
Wentao Zhao (Peking University)
Meng Wu (Peking University)
Le Ye (Peking University)
Ru Huang (Peking University)

Hardware Computation Graph for DNN Accelerator Design Automation without Inter-PU Templates

Jun Li (Nanjing University)
Wei Wang (Nanjing University)
Wu-Jun Li (Nanjing University)

Technical Program: Tuesday, November 1

6:00 AM – 7:00 AM, Virtual

4C Multi-purpose Fundamental Digital Design Improvements (Virtual)

Session Chair: Sabya Das (Synopsis)

Dynamic Frequency Boosting beyond Critical Path Delay

Nikolaos Zompakis (Trimsignal)

Sotirios Xydis (Harokopio University of Athens)

ASPPLN: Accelerated Symbolic Probability Propagation in Logic Network

Weihua Xiao (Shanghai Jiao Tong University)

Weikang Qian (Shanghai Jiao Tong University)

A High-precision Stochastic Solver for Steady-state Thermal Analysis with Fourier Heat Transfer Robin Boundary Conditions

Longlong Yang (Fudan University)

Cuiyang Ding (Fudan University)

Changhao Yan (Fudan University)

Dian Zhou (University of Texas at Dallas)

Xuan Zeng (Fudan University)

6:00 AM – 7:00 AM, Virtual

4D GPU Acceleration for Routing Algorithms (Virtual)

Session Chair: Umamaheswara Rao Tida (North Dakota State University)

Superfast Full-Scale GPU-Accelerated Global Routing

Shiju Lin (The Chinese University of Hong Kong)

Martin Wong (The Chinese University of Hong Kong)

X-Check: GPU-Accelerated Design Rule Checking via Parallel Sweep-line Algorithms

Zhuolun He (The Chinese University of Hong Kong)

Yuzhe Ma (The Hong Kong University of Science and Technology (Guangzhou))

Bei Yu (The Chinese University of Hong Kong)

GPU-Accelerated Rectilinear Steiner Tree Generation

Zizheng Guo (Peking University)

Feng Gu (Peking University)

Yibo Lin (Peking University)

Technical Program: Tuesday, November 1

7:10 AM – 8:30 AM, Virtual

5A Breakthroughs in Synthesis – Infrastructure and ML Assist I (Virtual)

Session Chair: Christian Pilato (Politecnico di Milano)

Session Co-Chair: Miroslav Velev (Aries Design Automation)

HECTOR: A Multi-level Intermediate Representation for Hardware Synthesis Methodologies

Ruifan Xu (Peking University)

Youwei Xiao (Peking University)

Jin Luo (Peking University)

Yun (Eric) Liang (Peking University)

QCIR: Pattern Matching Based Universal Quantum Circuit Optimization Framework

Mingyu Chen (University of Science and Technology of China)

Yu Zhang (University of Science and Technology of China)

YongShang Li (University of Science and Technology of China)

Zhen Wang (University of Science and Technology of China)

Jun Li (University of Science and Technology of China)

Xiang-Yang Li (University of Science and Technology of China)

Batch Sequential Black-box Optimization with Embedding Alignment Cells for Logic Synthesis

Chang Feng (Huawei Noah's Ark Lab)

Wenlong Lyu (Huawei Noah's Ark Lab)

Zhitang Chen (Huawei Noah's Ark Lab)

Junjie Ye (Huawei Noah's Ark Lab)

Mingxuan Yuan (Huawei Noah's Ark Lab)

Jianye Hao (Tianjin University)

Heterogeneous Graph Neural Network-based Imitation Learning for Gate Sizing Acceleration

Xinyi Zhou (The Chinese University of Hong Kong)

Junjie Ye (Huawei)

Chak-Wa Pui (Huawei)

Kun Shao (Huawei Noah's Ark Lab)

Guangliang Zhang (Huawei)

Bin Wang (Huawei)

Jianye Hao (Tianjin University)

Guangyong Chen (Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences)

Pheng Ann Heng (The Chinese University of Hong Kong)

Technical Program: Tuesday, November 1

7:10 AM – 7:50 AM, Virtual

5B Smart Search (Virtual)

Session Chair: Jianlei Yang (Beihang)

NASA: Neural Architecture Search and Acceleration for Hardware Inspired Hybrid Networks

Huihong Shi (Georgia Tech)

Haoran You (Georgia Tech)

Yang Zhao (Georgia Tech)

Zhongfeng Wang (Georgia Tech)

Yingyan Lin (Georgia Tech)

Personalized Heterogeneity-aware Federated Search Towards Better Accuracy and Energy Efficiency

Zhao Yang (Northwestern Polytechnical University)

Qingshuang Sun (Northwestern Polytechnical University)

7:10 AM – 7:50 AM, Virtual

5C Reconfigurable Computing: Accelerators and Methodologies I (Virtual)

Session Chair: Cheng Tan (Microsoft)

Towards High Performance and Accurate BNN Inference on FPGA with Structured Fine-Grained Pruning

Keqi Fu (Southeast University)

Zhi Qi (Southeast University)

Jiaxuan Cai (Southeast University)

Xulong Shi (Southeast University)

Towards High-Quality CGRA Mapping with Graph Neural Networks and Reinforcement Learning

Yan Zhuang (Chongqing University)

Zhihao Zhang (Chongqing University)

Dajiang Liu (Chongqing University)

Technical Program: Tuesday, November 1

7:10 AM – 7:50 AM, Virtual

5D Hardware Security: Attacks and Countermeasures (Virtual)

Session Chair: Johann Knechtel (NYU)

Session Co-Chair: Lejla Batina (Radboud University)

Attack Directories on ARM big.LITTLE Processors **Best Paper Award Nomination**

Zili Kou (Hong Kong University of Science and Technology)

Sharad Sinha (Indian Institute of Technology Goa)

Wenjian HE (Hong Kong University of Science and Technology)

Wei ZHANG (Hong Kong University of Science and Technology)

AntiSIFA-CAD: A Framework to Thwart SIFA at the Layout Level

Rajat Sadhukhan (Indian Institute of Technology Kharagpur)

Sayandeep Saha (School of Physical and Mathematical Sciences, NTU Singapore)

Debdeep Mukhopadhyay (Indian Institute of Technology Kharagpur)

Technical Program: Tuesday, November 1

9:00 AM – 10:30 AM, St. Tropez

6A Advanced VLSI Routing and Layout Learning

Session Chair: Wing-Kai Chow (Cadence Design Systems)

Session Co-Chair: David Chinnery (Siemens EDA)

A Stochastic Approach to Handle Non-Determinism in Deep Learning-Based Design Rule Violation Predictions

Rongjian Liang (NVIDIA)

Hua Xiang (IBM Research)

Jinwook Jung (IBM Research)

Jiang Hu (Texas A&M University)

Gi-Joon Nam (IBM Research)

Obstacle-Avoiding Multiple Redistribution Layer Routing with Irregular Structures

Yen-Ting Chen (National Taiwan University)

Yao-Wen Chang (National Taiwan University)

TAG: Learning Circuit Spatial Embedding from Layouts

Keren Zhu (University of Texas at Austin)

Hao Chen (University of Texas at Austin)

Walker Turner (NVIDIA Corporation)

George Kokai (NVIDIA Corporation)

Po-Hsuan Wei (NVIDIA Corporation)

David Z. Pan (University of Texas at Austin)

Haoxing Ren (NVIDIA Corporation)

Technical Program: Tuesday, November 1

9:00 AM – 10:30 AM, Monte Carlo

6B Physical Attacks and Countermeasures

Session Chair: Satwik Patnaik (TAMU)

Session Co-Chair: Gang Qu (UMD)

PowerTouch: A Security Objective-Guided Automation Framework for Generating Wired Ghost Touch Attack on Touchscreens

Huifeng Zhu (Washington University in St. Louis)

Zhiyuan Yu (Washington University in St. Louis)

Weidong Cao (Washington University in St. Louis)

Ning Zhang (Washington University in St. Louis)

Xuan Zhang (Washington University in St. Louis)

A Combined Logical and Physical Attack on Logic Obfuscation

Michael Zuzak (University of Maryland, College Park)

Yuntao Liu (University of Maryland, College Park)

Isaac McDaniel (University of Maryland, College Park)

Ankur Srivastava (University of Maryland, College Park)

A Pragmatic Methodology for Blind Hardware Trojan Insertion in Finalized Layouts

Alexander Hepp (Technical University of Munich)

Tiago Diadami Perez (Taltech)

Samuel Pagliarini (Tallinn University of Technology (TalTech))

Georg Sigl (Technical University of Munich/Fraunhofer AISEC)

9:00 AM – 10:30 AM, Riviera

6C Tutorial: Polynomial Formal Verification: Ensuring Correctness under Resource Constraints

Session Chair: Rolf Drechsler (University of Bremen/DFKI)

Polynomial Formal Verification: Ensuring Correctness under Resource Constraints

Rolf Drechsler (University of Bremen/DFKI)

Alireza Mahzoon (University of Bremen)

Technical Program: Tuesday, November 1

9:00 AM – 10:30 AM, Capri

6D Scalable Verification Technologies

Session Chair: Viraphol Chaiyakul (Belmont Computing)

Session Co-Chair: Alex Orailoglu (University of California, San Diego)

Arjun: An Efficient Independent Support Computation Technique and its Applications to Counting and Sampling

Mate Soos (National University of Singapore)

Kuldeep S Meel (National University of Singapore)

Compositional Verification Using a Formal Component and Interface Specification

Yue Xing (Princeton University)

Huaixi Lu (Princeton University)

Aarti Gupta (Princeton University)

Sharad Malik (Princeton University)

Usage-Based RTL Subsetting for Hardware Accelerators

Qinhan Tan (Princeton University)

Aarti Gupta (Princeton University)

Sharad Malik (Princeton University)

Technical Program: Tuesday, November 1

11:00 AM – 12:30 PM, St. Tropez

7A Optimizing Digital Design Aspects: From Gate Sizing to Multi-Bit Flip-Flops

Session Chair: Amit Gupta (AMD, Inc.)

Session Co-Chair: Dirk Stroobandt (UGent)

TransSizer: A Novel Transformer-Based Fast Gate Sizer [Best Paper Award Nomination](#)

Siddhartha Nath (NVIDIA Corp)

Geraldo Pradipta (NVIDIA Corp)

Corey Hu (NVIDIA Corp)

Tian Yang (NVIDIA Corp)

Brucek Khailany (NVIDIA Corp)

Haoxing Ren (NVIDIA Corp)

Generation of Mixed-Driving Multi-Bit Flip-Flops for Power Optimization

Meng-Yun Liu (National Tsing Hua University)

Yu-Cheng Lai (National Tsing Hua University)

Wai-Kei Mak (National Tsing Hua University)

Ting-Chi Wang (National Tsing Hua University)

DEEP: Developing Extremely Efficient Runtime On-Chip Power Meters

Zhiyao Xie (Hong Kong University of Science and Technology)

Shiyu Li (Duke University)

Mingyuan Ma (Duke University)

Chen-Chia Chang (Duke University)

Jingyu Pan (Duke University)

Yiran Chen (Duke University)

Jiang Hu (Texas A&M University)

Technical Program: Tuesday, November 1

11:00 AM – 12:30 PM, Monte Carlo

7B Energy Efficient Hardware Acceleration and Stochastic Computing

Session Chair: Sunil Khatri (TAMU)

Session Co-Chair: Anish Krishnakumar (U of Wisconsin)

ReD-LUT: Reconfigurable In-DRAM LUTs Enabling Massive Parallel Computation

Ranyang Zhou (New Jersey Institute of Technology)

Arman Roohi (University of Nebraska – Lincoln)

Durga Misra (New Jersey Institute of Technology)

Shaahin Angizi (New Jersey Institute of Technology)

Sparse-T: Hardware accelerator thread for unstructured sparse data processing

Pranathi Vasireddy (University of North Texas)

Krishna Kavi (University of North Texas)

Gayatri Mehta (University of North Texas)

Sound Source Localization using Stochastic Computing

Peter Schober (TU Wien)

Seyedeh Newsha Estiri (University of Louisiana at Lafayette)

Sercan Aygun (University of Louisiana at Lafayette)

Nima TaheriNejad (TU Wien)

M. Hassan Najafi (University of Louisiana at Lafayette)

11:00 AM – 12:30 PM, Riviera

7C Special Session: Approximate Computing and the Efficient Machine Learning Expedition

Session Chair: Medhi Tahoori (Karlsruhe Institute of Technology)

Approximate Computing and the Efficient Machine Learning Expedition

Approximate Computing and ML: A match made in heaven

Efficient Processing-in-Memory Design for Transformer-based Models

Extremely Resource Constrained ML Inference via Approximation and Codesign

Jörg Henkel (Karlsruhe Institute of Technology)

Hai Li (Duke University)

Anand Raghunathan (Purdue University)

Mehdi Tahoori (Karlsruhe Institute of Technology)

Swagath Venkataramani (IBM Research)

Xiaoxuan Yang (Duke University)

Georgios Zervakis (Karlsruhe Institute of Technology)

Technical Program: Tuesday, November 1

11:00 AM – 12:30 PM, Capri

7D Co-search Methods and Tools

Session Chair: Cunxi Yu (University of Utah)

Session Co-Chair: Yingyan “Celine” Lin (Georgia Tech)

ObfuNAS: A Neural Architecture Search-based DNN Obfuscation Approach [Best Paper Award Nomination](#)

Tong Zhou (Northeastern University)

Shaolei Ren (UC Riverside)

Xiaolin Xu (Northeastern University)

Deep Learning Toolkit-Accelerated Analytical Co-optimization of CNN Hardware and Dataflow

Rongjian Liang (NVIDIA)

Jianfeng Song (Texas A&M University)

Bo Yuan (Rutgers University)

Jiang Hu (Texas A&M University)

HD Torch: Accelerating Hyperdimensional Computing with GP-GPUs for Design Space Exploration

William Simon (École Polytechnique Fédérale de Lausanne)

Una Pale (Swiss Federal Institute of Technology, Lausanne)

Tomas Teijeiro (University of the Basque Country UPV/EHU)

David Atienza (École Polytechnique Fédérale de Lausanne (EPFL))

2:00 PM – 3:00 PM, St. Tropez

8A Reconfigurable Computing: Accelerators and Methodologies II

Session Chair: Peipei Zhou (University of Pittsburgh)

DARL: Distributed Reconfigurable Accelerator for Hyperdimensional Reinforcement Learning

Hanning Chen (University of California, Irvine)

Mariam Issa (University of California, Irvine)

Yang Ni (University of California, Irvine)

Mohsen Imani (University of California Irvine)

Temporal Vectorization: A Compiler Approach to Automatic Multi-Pumping

Carl-Johannes Johnsen (University of Copenhagen)

Tiziano De Matteis (ETH Zurich)

Tal Ben-Nun (ETH Zurich)

Johannes de Fine Licht (ETH Zurich)

Torsten Hoeffler (ETH Zurich)

Technical Program: Tuesday, November 1

2:00 PM – 3:00 PM, Monte Carlo

8B Compute-in-Memory for Neural Networks

Session Chair: Bo Yuan (Rutgers University)

ISSA: Input-Skippable, Set-Associative Computing-in-Memory (SA-CIM) Architecture for Neural Network Accelerators

Yun-Chen Lo (National Tsing Hua University)

Chih-Chen Yeh (National Tsing Hua University)

Jun-Shen Wu (National Tsing Hua University)

Chia-Chun Wang (National Tsing Hua University)

Yu-Chih Tsai (National Tsing Hua University)

Wen-Chien Ting (National Tsing Hua University)

Ren-Shuo Liu (National Tsing Hua University)

Computing-In-Memory Neural Network Accelerators for Safety-Critical Systems: Can Small Weight Variations Be Disastrous?

Zheyu Yan (University of Notre Dame)

X. Sharon Hu (University of Notre Dame)

Yiyu Shi (University of Notre Dame)

2:00 PM – 3:00 PM, Riviera

8C Breakthroughs in Synthesis – Infrastructure and ML Assist II

Session Chair: Sunil Khatri (Texas A&M University)

Session Co-Chair: Cunxi Yu (The University of Utah)

Language Equation Solving via Boolean Automata Manipulation

Wan-Hsuan Lin (National Taiwan University)

Chia-Hsuan Su (National Taiwan University)

Jie-Hong Roland Jiang (National Taiwan University)

How Good is Your Verilog RTL Code? A Quick Answer from Machine Learning

Prianka Sengupta (Texas A&M University)

Aakash Tyagi (Texas A&M University)

Yiran Chen (Duke University)

Jiang Hu (Texas A&M University)

Technical Program: Tuesday, November 1

2:00 PM – 3:00 PM, Capri

8D In-Memory Computing Revisited

Session Chair: Biresh Kumar Joardar (University of Houston)

Session Co-Chair: Ulf Schlichtmann (Technical University of Munich)

Logic Synthesis for Digital In-Memory Computing **Best Paper Award Nomination**

Muhammad Rashedul Haq Rashed (University of Central Florida)

Sumit Kumar Jha (University of Texas at San Antonio)

Rickard Ewetz (University of Central Florida)

Design Space and Memory Technology Co-exploration for In-Memory Computing Based Machine Learning Accelerators

Kang He (Purdue University)

Indranil Chakraborty (Purdue University)

Cheng Wang (Purdue University)

Kaushik Roy (Purdue University)

Technical Program: Tuesday, November 1

3:30 PM – 5:30 PM, St. Tropez

9A Special Session: 2022 CAD contest at ICCAD

Session Chair: Yu-Guang Chen (National Central University)

Overview of 2022 CAD contest at ICCAD

Yu-Guang Chen (National Central University)

Chun-Yao Wang (National Tsing Hua University)

Tsung-Wei Huang (University of Utah)

Takashi Sato (Kyoto University)

2022 ICCAD CAD Contest Problem A: Learning Arithmetic Operations from Gate-Level Circuit

Chung-Han Chou (Cadence Taiwan, Inc.)

Chih-Jen (Jacky) Hsu (Cadence Taiwan, Inc.)

Chi-An (Rocky) Wu (Cadence Taiwan, Inc.)

Kuan-Hua Tu (Cadence Taiwan, Inc.)

2022 ICCAD CAD Contest Problem B: 3D Placement with D2D Vertical Connections

Kai-Shun Hu (Synopsys, Inc.)

I-Jye Lin (Synopsys, Inc.)

Yu-Hui Huang (Synopsys, Inc.)

Hao-Yu Chi (Synopsys, Inc.)

Yi-Hsuan Wu (Synopsys, Inc.)

Chin-Fang Cindy Shen (Synopsys, Inc.)

2022 ICCAD CAD Contest Problem C: Microarchitecture Design Space Exploration

Sicheng Li (Alibaba Group)

Chen Bai (Alibaba Group)

Xuechao Wei (Alibaba Group)

Bizhao Shi (Alibaba Group)

Yen-Kuang Chen (Alibaba Group)

Yuan Xie (Alibaba Group)

IEEE CEDA DATC: Expanding Research Foundations for IC Physical Design and ML-Enabled EDA

Jinwook Jung (IBM Research)

Andrew Kahng (University of California, San Diego)

Ravi Varadarajan (University of California, San Diego)

Zhiang Wang (University of California, San Diego)

Technical Program: Tuesday, November 1

3:30 PM – 5:30 PM, Monte Carlo

9B Architectures and Methodologies for Advanced Hardware Security

Session Chair: Amin Rezaei (California State University Long Beach)

Session Co-Chair: Gang Qu (UMD)

Inhale: Enabling High-Performance and Energy-Efficient In-SRAM Cryptographic Hash for IoT

Jingyao Zhang (University of California, Riverside)

Elaheh Sadredini (University of California, Riverside)

Accelerating N-bit Operations over TFHE on Commodity CPU-FPGA

Kevin Nam (Seoul National University)

Hyunyoung Oh (Gachon University)

Hyungon Moon (UNIST)

Yunheung Paek (Seoul National University)

Fast and Compact Interleaved Modular Multiplication based on Carry Save Addition

Oleg Mazonka (New York University Abu Dhabi)

Eduardo Chielle (New York University Abu Dhabi)

Deepraj Soni (New York University Tandon School of Engineering)

Michail Maniatakos (New York University Abu Dhabi)

Accelerating Fully Homomorphic Encryption by Bridging Modular and Bit-Level Arithmetic

Eduardo Chielle (New York University Abu Dhabi)

Oleg Mazonka (New York University Abu Dhabi)

Homer Gamil (New York University Abu Dhabi)

Michail Maniatakos (New York University Abu Dhabi)

Technical Program: Tuesday, November 1

3:30 PM – 5:30 PM, Riviera

9C Special Session: The Dawn of Domain-specific Hardware Accelerators for Robotic Computing

Session Chair: Dr. Jiang Hu (Texas A&M University)

A Reconfigurable Hardware Library for Robot Scene Perception

Yanqi Liu (Brown University)

Anthony Pipari (University of Michigan)

Odest Chadwicke Jenkins (University of Michigan)

R. Iris Bahar (Colorado School of Mines)

Analyzing and Improving Resilience and Robustness of Autonomous Systems

Zishen Wan (Georgia Institute of Technology)

Karthik Swaminathan (IBM T.J. Watson Research Center)

Pin-Yu Chen (IBM T.J. Watson Research Center)

Nandhini Chandramoorthy (IBM T.J. Watson Research Center)

Arijit Raychowdhury (Georgia Institute of Technology)

Factor Graph Accelerator for LiDAR-Inertial Odometry

Yuhui Hao (Tianjin University)

Bo Yu (PerceptIn)

Qiang Liu (Tianjin University)

Shaoshan Liu (PerceptIn)

Yuhao Zhu (University of Rochester)

Hardware Architecture of Graph Neural Network-enabled Motion Planner

Lingyi Huang (Rutgers University)

Xiao Zang (Rutgers University)

Yu Gong (Rutgers University)

Bo Yuan (Rutgers University)

Technical Program: Tuesday, November 1

3:30 PM – 5:30 PM, Capri

9D From logical to physical qubits: new models and techniques for mapping

Session Chair: Weiwen Jiang (George Mason University)

A Robust Quantum Layout Synthesis Algorithm with a Qubit Mapping Checker

Tsou-An Wu (National Taiwan University of Science and Technology)

Yun-Jhe Jiang (National Taiwan University of Science and Technology)

Shao-Yun Fang (National Taiwan University of Science and Technology)

Reinforcement Learning and DEAR Framework for Solving the Qubit Mapping Problem

Ching-Yao Huang (National Tsing Hua University)

Chi Hsiang Lien (National Tsing Hua University)

Wai-Kei Mak (National Tsing Hua University)

Qubit Mapping for Reconfigurable Atom Arrays

Bochen Tan (University of California, Los Angeles)

Dolev Bluvstein (Harvard University)

Jason Cong (University of California, Los Angeles)

Mikhail Lukin (Harvard University)

MCQA: Multi-Constraint Qubit Allocation for Near-FTQC Device

Sunghye Park (Pohang University of Science and Technology)

Dohun Kim (Pohang University of Science and Technology)

Jae-Yoon Sim (Pohang University of Science and Technology)

Seokhyeong Kang (Pohang University of Science and Technology)

ACM/IEEE EDA Job Fair

Our in-person meetings are Nov. 1st (Tuesday) 5:30 PM PT! Location: Terazza Ballroom, SAN DIEGO MISSION BAY RESORT. Join and enjoy the dinner from ACM SIGDA. We are planning to have an online session on Nov. 2nd! ACM SIGDA and IEEE CEDA will be holding their annual (1st) EDA job fair at the 2022 International Conference on Computer-Aided Design (ICCAD) conference, in-person, on November 1st (5:30 PM—7:30 PM PDT) in San Diego CA, as well as online, on November 2nd (6:00—7:00 AM PDT). The job fair is open to all attendees of the ICCAD conference. Attendees are encouraged to submit a CV or résumé for circulation beforehand. The EDA job fair is a place for students and professionals looking for internships or jobs to meet with representatives from companies and academia. In the beginning of the event, one representative from each organization has the opportunity to introduce the organization and its job opening(s). Afterward, all attendees have a chance to mingle. If you are representing a company, research organization or university and would like to participate in the job fair, please send an email with your contact information to sigdajobfair@gmail.com. In addition, all job fair participants must register (at least one-day) for the ICCAD.

Participating Companies

- Infineon Technologies AG
- Futurewei technologies
- NVIDIA
- Pacific Northwest National Laboratory (PNNL)
- MediaTek
- Zero ASIC
- Cadence
- Synopsys
- More to come!!

*Names in no particular order

Submit Your CV

As part of the job fair, attendees are encouraged to submit their CV to all of the participating companies before the job fair. This will help companies identify and possibly schedule an onsite interview with you when you attend. Please clearly indicate on your CV or résumé your availability and type of job interest, along with contact information! By uploading your CV, you are agreeing to be contacted by participating and sponsor companies about recruiting and job openings.

Organizers

Chair, Jeff (Jun) Zhang, Assistant Professor, Arizona State University

Co-chair, Mimi Xie, Assistant Professor, University of Texas at San Antonio

SIGDA Education Chair, Jingtong Hu, Associate Professor, University of Pittsburgh

CEDA VP Technical Activities, Tsung-Yi Ho, Professor, The Chinese University of Hong Kong

Sponsors

ACM Special Interest Group on Design Automation (SIGDA)

IEEE Council on Electronic Design Automation (CEDA)

International Conference on Computer-Aided Design (ICCAD)

Technical Program: Wednesday, November 2

6:00 AM – 7:00 AM, Virtual

10A Smart Embedded Systems (Virtual)

Session Chair: Leonidas Kosmidis (Barcelona Supercomputing Center)

Session Co-Chair: Pietro Mercati (Intel Labs)

Smart Scissor: Coupling Spatial Redundancy Reduction and CNN Compression for Embedded Hardware

Hao Kong (Nanyang Technological University)

Di Liu (Nanyang Technological University)

Shuo Huai (Nanyang Technological University)

Xiangzhong Luo (Nanyang Technological University)

Weichen Liu (Nanyang Technological University)

Ravi Subramaniam (HP Inc.)

Christian Makaya (HP Inc.)

Qian Lin (HP Inc.)

SHAPE: Scheduling of Fixed-Priority Tasks on Heterogeneous Architectures with Multi CPUs and Many PEs

Yuankai Xu (Shanghai Jiao Tong University)

Tiancheng He (Shanghai Jiao Tong University)

Ruiqi Sun (Shanghai Jiao Tong University)

Yehan Ma (Shanghai Jiao Tong University)

Yier Jin (University of Florida)

An Zou (Shanghai Jiao Tong University)

On Minimizing the Read Latency of Flash Memory to Preserve Inter-tree Locality in Random Forest

Yu-Cheng Lin (National Tsing Hua University)

Yu-Pei Liang (Chung Cheng University)

Tseng-Yi Chen (National Central University)

Yuan-Hao Chang (Academia Sinica)

Shuo-Han Chen (National Taipei University of Technology)

Wei-Kuan Shih (National Tsing Hua University)

Technical Program: Wednesday, November 2

6:00 AM – 7:00 AM, Virtual

10B Analog/Mixed-Signal Simulation, Layout, and Packaging (Virtual)

Session Chair: Biying Xu (Cadence)

Session Co-Chair: Ilya Yusim (Cadence)

Numerically-Stable and Highly-Scalable Parallel LU Factorization for Circuit Simulation

Xiaoming Chen (Institute of Computing Technology, Chinese Academy of Sciences)

EI-MOR: A Hybrid Exponential Integrator and Model Order Reduction Approach for Transient Power/Ground Network Analysis

Cong Wang (Southern University of Science and Technology)

Dongen Yang (Southern University of Science and Technology)

Quan Chen (Southern University of Science and Technology)

Multi-Package Co-Design for Chiplet Integration

Zhen Zhuang (The Chinese University of Hong Kong)

Bei Yu (The Chinese University of Hong Kong)

Kai-Yuan Chao (Hong Kong Research Center, Huawei Technology Investment Co. Ltd.)

Tsung-Yi Ho (The Chinese University of Hong Kong)

Technical Program: Wednesday, November 2

6:00 AM – 7:00 AM, Virtual

10C Advanced PIM and Biochip Technology and Stochastic Computing (Virtual)

Session Chair: Grace Li Zhang (TUM)

Gzippo: Highly-compact Processing-In-Memory Graph Accelerator Alleviating Sparsity and Redundancy

Xing Li (Shanghai Jiao Tong University)

Rachata Ausavarungrun (King Mongkut's University of Technology North Bangkok)

Xiao Liu (Bytedance Inc)

Xueyuan Liu (Shanghai Jiao Tong University)

Xuan Zhang (Shanghai Jiao Tong University)

Heng Lu (Shanghai Jiao Tong University)

Zhuoran Song (Shanghai Jiao Tong University)

Naifeng Jing (Shanghai Jiao Tong University)

Xiaoyao Liang (Shanghai Jiao Tong University)

CoMUX: Combinatorial-Coding-Based High-Performance Microfluidic Control Multiplexer Design

Siyuan Liang (The Chinese University of Hong Kong (CUHK))

Mengchu Li (Technical University of Munich)

Tsun-Ming Tseng (Technical University of Munich)

Ulf Schlichtmann (Technical University of Munich)

Tsung-Yi Ho (The Chinese University of Hong Kong)

Exploiting Uniform Spatial Distribution to Design Efficient Random Number Source for Stochastic Computing

Kuncui Zhong (Shanghai Jiao Tong University)

Zexi Li (Shanghai Jiao Tong University)

Haoran Jin (Shanghai Jiao Tong University)

Weikang Qian (Shanghai Jiao Tong University)

Technical Program: Wednesday, November 2

6:00 AM – 6:40 AM, Virtual

10D On Automating Heterogeneous Designs (Virtual)

Session Chair: Haocheng Li (Cadence)

A Novel Blockage-avoiding Macro Placement Approach for 3D ICs based on POCS

Jai-Ming Lin (National Cheng Kung University)

Po-Chen Lu (National Cheng Kung University)

Heng-Yu Lin (National Cheng Kung University)

Jia-Ting Tsai (National Cheng Kung University)

Routability-driven Analytical Placement with Precise Penalty Models for Large-Scale 3D ICs

Jai-Ming Lin (National Cheng Kung University)

Hao-Yuan Hsieh (National Cheng Kung University)

Hsuan Kung (National Cheng Kung University)

Hao-Jia Lin (National Cheng Kung University)

7:10 AM – 8:30 AM, Virtual

11A Special Session: Quantum Computing to Solve Chemistry, Physics and Security Problems (Virtual)

Session Chair: Swaroop Ghosh (Penn State University)

Developing Scalable Algorithms to Inform Co-Design

Anne Matsuura (Intel Corporation)

Quantum Machine Learning Applications in High-Energy Physics

Andrea Delgado (Oak Ridge National Laboratory)

Kathleen Hamilton (Oak Ridge National Laboratory)

Quantum Machine Learning for Material Synthesis and Hardware Security

Collin Beaudoin (Pennsylvania State University)

Satwik Kundu (Pennsylvania State University)

Rasit Topaloglu (IBM)

Swaroop Ghosh (Pennsylvania State University)

Technical Program: Wednesday, November 2

7:10 AM – 8:30 AM, Virtual

11B Making Patterning Work (Virtual)

Session Chair: Yuzhe Ma (Hong Kong University of Science and Technology (Guangzhou))

DeePEB: A Neural Partial Differential Equation Solver for Post Exposure Baking Simulation in Lithography **Best Paper Award Nomination**

Qipan Wang (Peking University)

Xiaohan Gao (Peking University)

Yibo Lin (Peking University)

Runsheng Wang (Peking University)

Ru Huang (Peking University)

AdaOPC: A Self-Adaptive Mask Optimization Framework For Real Design Patterns

Wenqian Zhao (The Chinese University of Hong Kong)

Xufeng Yao (The Chinese University of Hong Kong)

Ziyang Yu (The Chinese University of Hong Kong)

Guojin Chen (The Chinese University of Hong Kong)

Yuzhe Ma (The Hong Kong University of Science and Technology (Guangzhou))

Bei Yu (The Chinese University of Hong Kong)

Martin Wong (The Chinese University of Hong Kong)

LayoutTransformer: Generating Layout Patterns with Transformer via Sequential Pattern Modeling

Liangjian Wen (Huawei Technologies)

Yi Zhu (Huawei Technologies)

Lei Ye (Huawei Technologies)

Guojin Chen (The Chinese University of Hong Kong)

Bei Yu (The Chinese University of Hong Kong)

Jianzhuang Liu (Huawei Noah's Ark Lab)

Chunjing Xu (Huawei Technologies)

WaferHSL: Wafer Failure Pattern Classification with Efficient Human-Like Staged Learning

Qijing Wang (The Chinese University of Hong Kong)

Martin Wong (The Chinese University of Hong Kong)

Technical Program: Wednesday, November 2

7:10 AM – 7:50 AM, Virtual

11C Advanced Verification Technologies (Virtual)

Session Chair: Takahide Yoshikawa (Fujitsu)

Combining Bounded Model Checking and Complementary Approximate Reachability to Accelerate Bug-Finding

Xiaoyu Zhang (East China Normal University)

Shengping Xiao (East China Normal University)

Jianwen Li (East China Normal University)

Geguang Pu (East China Normal University)

Ofer Strichman (Israel Institute of Technology)

Equivalence Checking of Dynamic Quantum Circuits

Xin Hong (University of Technology Sydney)

Yuan Feng (University of Technology Sydney)

Sanjiang Li (University of Technology Sydney)

Mingsheng Ying (Institute of Software, Chinese Academy of Sciences)

7:10 AM – 7:50 AM, Virtual

11D Routing with Cell Movement (Virtual)

Session Chair: Guojie Luo (Peking University)

ATLAS: A Two-Level Layer-Aware Scheme for Routing with Cell Movement

Xinshi Zang (The Chinese University of Hong Kong)

Fangzhou Wang (The Chinese University of Hong Kong)

Jinwei Liu (The Chinese University of Hong Kong)

Martin Wong (The Chinese University of Hong Kong)

A Robust Global Routing Engine with High-accuracy Cell Movement under Advanced Constraints

Ziran Zhu (National ASIC System Engineering Center, Southeast University)

Fuheng Shen (National ASIC System Engineering Center, Southeast University)

Yangjie Mei (National ASIC System Engineering Center, Southeast University)

Zhipeng Huang (Peng Cheng Laboratory)

Jianli Chen (State Key Lab of ASIC & System, Fudan University)

Jun Yang (National ASIC System Engineering Center, Southeast University)

Technical Program: Wednesday, November 2

10:30 AM – 12:30 PM, St. Tropez

12A Special Session: Hardware Security Through Reconfigurability: Attacks, Defenses, and Challenges

Session Chair: Michael Raitza (TU Dresden)

Securing Hardware through Reconfigurable Nano-structures

Nima Kavand (TU Dresden)

Armin Darjani (TU Dresden)

Shubham Rai (TU Dresden)

Akash Kumar (TU Dresden)

Reconfigurable Logic for Hardware IP Protection: Opportunities and Challenges

Luca Collini (New York University)

Benjamin Tan (University of Calgary)

Christian Pilato (Politecnico di Milano)

Ramesh Karri (New York University)

Towards Security-Adaptive Hardware: A Hitchhiker's Guide

Patrick Jauernig (TU Darmstadt)

Emmanuel Stapf (TU Darmstadt)

Ahmad-Reza Sadeghi (TU Darmstadt)

Jeyavijayan Rajendran (Texas A&M University)

Enabling Systematic and Measurable Security Verification

Jason Oberg (Tortuga Logic)

Andres Meza (UC San Diego)

Ryan Kastner (UC San Diego)

Technical Program: Wednesday, November 2

10:30 AM – 12:30 PM, Monte Carlo

12B Performance, Power and Temperature Aspects in Deep Learning

Session Chair: Callie Hao (Georgia Tech)

Session Co-Chair: Jeff Zhang (ASU)

RT-NeRF: Real-Time On-Device Neural Radiance Fields Towards Immersive AR/VR Rendering

Chaojian Li (Georgia Tech)

Sixu Li (Georgia Tech)

Yang Zhao (Georgia Tech)

Wenbo Zhu (Georgia Tech)

Yingyan Lin (Georgia Tech)

All-in-One: A Highly Representative DNN Pruning Framework for Edge Devices with Dynamic Power Management

Yifan Gong (Northeastern University)

Zheng Zhan (Northeastern University)

Pu Zhao (Northeastern.edu)

Yushu Wu (Northeastern University)

Chao Wu (Northeastern University)

Caiwen Ding (University of Connecticut)

Weiwen Jiang (George Mason University)

Minghai Qin (Self-employed)

Yanzhi Wang (Northeastern University)

Robustify ML-based Lithography Hotspot Detectors

Jingyu Pan (Duke University)

Chen-Chia Chang (Duke University)

Zhiyao Xie (Hong Kong University of Science and Technology)

Jiang Hu (Texas A&M University)

Yiran Chen (Duke University)

Associative Memory Based Experience Replay for Deep Reinforcement Learning

Mengyuan Li (University of Notre Dame)

Arman Kazemi (University of Notre Dame)

Ann Franchesca Laguna (University of Notre Dame)

X. Sharon Hu (University of Notre Dame)

Technical Program: Wednesday, November 2

10:30 AM – 12:30 PM, Riviera

12C Tutorial: TorchQuantum Case Study for Robust Quantum Circuits

Session Chair: Hanrui Wang (MIT)

TorchQuantum Case Study for Robust Quantum Circuits

Hanrui Wang (Massachusetts Institute of Technology)

Zhiding Liang (University of Notre Dame)

Jiaqi Gu (The University of Texas at Austin)

Zirui Li (SJTU)

Yongshan Ding (Yale University)

Weiwen Jiang (George Mason University)

Yiyu Shi (University of Notre Dame)

David Z. Pan (University of Texas at Austin)

Frederic T. Chong (The University of Chicago)

Song Han (Massachusetts Institute of Technology)

Technical Program: Wednesday, November 2

10:30 AM – 12:30 PM, Capri

12D Emerging Machine Learning Primitives: From Technology to Application

Session Chair: Dharanidhar Dang (UC San Diego)

Session Co-Chair: Yiran Chen (Duke University)

COSIME: FeFET based Associative Memory for In-Memory Cosine Similarity Search

Che-Kai Liu (Zhejiang University)

Haobang Chen (Zhejiang University)

Mohsen Imani (University of California Irvine)

Kai Ni (RIT)

Arman Kazemi (University of Notre Dame)

Ann Franchesca Laguna (University of Notre Dame)

Michael Niemier (University of Notre Dame)

X. Sharon Hu (University of Notre Dame)

Liang Zhao (Zhejiang University)

Cheng Zhuo (Zhejiang University)

Xunzhao Yin (Zhejiang University)

DynaPAT: A Dynamic Pattern-Aware Encoding Technique for Robust MLC PCM-Based Deep Neural Networks

Thai Hoang Nguyen (Sungkyunkwan University)

Muhammad Imran (National University of Sciences and Technology)

Joon-Sung Yang (Yonsei University)

Graph Neural Networks for Idling Error Mitigation

Vedika Saravanan (City College of New York)

Samah Saeed (City College of New York)

Quantum Neural Network Compression

Zhirui Hu (George Mason University)

Peiyan Dong (Northeastern University)

Zhepeng Wang (George Mason University)

Youzuo Lin (Los Alamos National Laboratory)

Yanzhi Wang (Northeastern University)

Weiwen Jiang (George Mason University)

Technical Program: Wednesday, November 2

1:45 PM – 3:15 PM, St. Tropez

13A Design for Low Energy, Low Resource, but High Quality

Session Chair: Ravikumar Chakaravarthy (Xilinx)

Session Co-Chair: Cong “Callie” Hao (Georgia Tech)

Squeezing Accumulators in Binary Neural Networks for Extremely Resource-Constrained Applications

Azat Azamat (Ulsan National Institute of Science and Technology)

Jaewoo Park (Ulsan National Institute of Science and Technology)

Jongeun Lee (Ulsan National Institute of Science and Technology)

WSQ-AdderNet: Efficient Weight Standardization based Quantized AdderNet FPGA Accelerator Design with High-Density INT8 DSP-LUT Co-Packing Optimization

Yunxiang Zhang (Binghamton University)

Biao Sun (Tianjin University)

Weixiong Jiang (ShanghaiTech University)

Yajun Ha (ShanghaiTech University)

Miao Hu (TetraMem Inc.)

Wenfeng Zhao (Binghamton University)

Low-Cost 7T-SRAM Compute-In-Memory design based on Bit-Line Charge-Sharing based Analog-To-Digital Conversion

Kyeongho Lee (Korea University)

Joonhyung Kim (Korea University)

Jongsun Park (Korea University)

Technical Program: Wednesday, November 2

1:45 PM – 3:15 PM, Monte Carlo

13B Microarchitectural Attacks and Countermeasures

Session Chair: Rajesh JS (Intel)

Session Co-Chair: Amin Rezaei (California State University Long Beach)

Speculative Load Forwarding Attack on Modern Processors

Hasini Witharana (University of Florida)

Prabhat Mishra (University of Florida)

Fast, Robust and Accurate Detection of Cache-based Spectre Attack Phases

Arash Pashrashid (National University of Singapore)

Ali Hajiabadi (National University of Singapore)

Trevor E. Carlson (National University of Singapore)

CASU: Compromise Avoidance via Secure Updates for Low-end Embedded Systems

Ivan De Oliveira Nunes (Rochester Institute of Technology)

Sashidhar Jakkamsetti (UC Irvine)

Youngil Kim (UC Irvine)

Gene Tsudik (UC Irvine)

1:45 PM – 3:15 PM, Riviera

13C Genetic Circuits meet Ising Machines

Session Chair: Marc Riedel (University of Minnesota)

Session Co-Chair: Lei Yang (George Mason University)

Technology Mapping of Genetic Circuits: From Optimal to Fast Solutions

Tobias Schwarz (TU Darmstadt)

Christian Hochberger (TU Darmstadt)

DaS: Implementing Dense Ising Machines Using Sparse Resistive Networks

Naomi Sagan (University of California, Berkeley)

Jaijeet Roychowdhury (University of California, Berkeley)

QuBRIM: A CMOS Compatible Resistively-coupled Ising Machine with Quantized Nodal Interactions

Yiqiao Zhang (University of Rochester)

Uday Kumar Reddy Vengalam (University of Rochester)

Anshujit Sharma (University of Rochester)

Michael Huang (University of Rochester)

Zeljko Ignjatovic (University of Rochester)

TinyML Design Contest

ACM/IEEE TinyML Design Contest at ICCAD is a challenging, multi-month, research and development competition, focusing on real-world problems that requires the implementation of machine learning algorithms on low-end microprocessors/microcontrollers. It is open to multi-person teams world-wide. The top three teams will be invited to 2022 International Conference on Computer-Aided Design (ICCAD) to present their solutions, and to receive their awards.

Winner Announced

1:45-3:15 pm at Capri on November 2 at ICCAD

Awards

1st Place Award
US \$4500 / team
2nd Place Award
US \$1500 / team
3rd Place Award
US \$500 / team

Contest Organizers

Zhenge Jia (University of Notre Dame, IN, US)
Dawei Li (South-Central Minzu University, CN)
Lichuan Ping (Singular Medical, CN)
Yiyu Shi (University of Notre Dame, IN, US)

Technical Program: Wednesday, November 2

3:45 PM – 5:45 PM, St. Tropez

14A Energy Efficient Neural Networks Via Approximate Computations

Session Chair: M. Hasan Najafi (University of Louisiana at Lafayette)

Session Co-Chair: Vidya Chabria (University of Minnesota)

Combining Gradients and Probabilities for Heterogeneous Approximation of Neural Networks

Elias Trommer (Infineon Technologies)

Bernd Waschneck (Infineon Technologies)

Akash Kumar (Technische Universitaet Dresden)

Tunable Precision Control for Approximate Image Filtering in an In-Memory Architecture with Embedded Neurons

Ayushi Dube (Arizona State University)

Ankit Wagle (Arizona State University)

Gian Singh (Arizona State University)

Sarma Vrudhula (Arizona State University)

AppGNN: Approximation-Aware Functional Reverse Engineering using Graph Neural Networks

Tim Bücher (University of Stuttgart)

Lilas Alrahis (New York University Abu Dhabi)

Guilherme Paim (INESC-ID)

Sergio Bampi (Federal Univ. of Rio Grande do Sul)

Ozgur Sinanoglu (New York University Abu Dhabi)

Hussam Amrouch (University of Stuttgart)

Seprox: Sequence-based Approximations for Compressing Ultra-Low Precision Deep Neural Networks

Aradhana Mohan Parvathy (Purdue University)

Sarada Krithivasan (Purdue University)

Sanchari Sen (IBM T.J. Watson Research Center)

Anand Raghunathan (Purdue University)

Technical Program: Wednesday, November 2

3:45 PM – 5:45 PM, Monte Carlo

14B Algorithms and Tools for Security Analysis and Secure Hardware Design

Session Chair: Rosario Cammarota (Intel)

Session Co-Chair: Satwik Patnaik (TAMU)

Evaluating the Security of eFPGA-based Redaction Algorithms

Amin Rezaei (California State University, Long Beach)

Raheel Afsharmazayejani (University of Calgary)

Jordan Maynard (California State University, Long Beach)

An Approach to Unlocking Cyclic Logic Locking – LOOPLock 2.0

Pei-Pei Chen (National Tsing Hua University)

Xiang-Min Yang (National Tsing-Hua University)

Yi-Ting Li (National Tsing Hua University)

Yung-Chih Chen (National Taiwan University of Science and Technology)

Chun-Yao Wang (National Tsing Hua University)

Garbled EDA: Privacy Preserving Electronic Design Automation

Mohammad Hashemi (Worcester Polytechnic Institute)

Steffi Roy (University of Florida)

Fatemeh Ganji (Worcester Polytechnic Institute)

Domenic Forte (University of Florida)

Don't CWEAT It: Toward (CWE) (A)nalysis (T)echniques in Early Stages of Hardware Design

Baleegh Ahmad (New York University)

Wei-Kai Liu (Duke University)

Luca Collini (New York University)

Hammond Pearce (New York University)

Jason Fung (Intel)

Jonathan Valamehr (Intel)

Mohammad Bidmeshki (Intel)

Piotr Sapienza (Intel)

Steve Brown (Intel)

Krishnendu Chakrabarty (Duke University)

Ramesh Karri (New York University)

Benjamin Tan (University of Calgary)

Technical Program: Wednesday, November 2

3:45 PM – 5:45 PM, Riviera

14C Special Session: Making ML Reliable: From Devices to Systems to Software

Session Chair: Krishnendu Chakrabarty (Duke University)

Session Co-Chair: Partha Pande (Washington State University)

Reliable Computing of ReRAM Based Compute-in-Memory Circuits for AI Edge Devices

Meng-Fan Chang (National Tsing Hua University)

Je-Ming Hung (National Tsing Hua University)

Ping-Cheng Chen (I-Shou University)

Tai-Hao Wen (National Tsing Hua University)

Fault-tolerant Deep Learning Using Regularization

Biresk Kumar Joardar (University of Houston)

Aqeeb Iqbal Arka (Washington State University)

Janardhan Rao Doppa (Washington State University)

Partha Pratim Pande (Washington State University)

Machine Learning for Testing Machine-Learning Hardware: A Virtuous Cycle

Arjun Chaudhuri (Duke University)

Jonti Talukdar (Duke University)

Krishnendu Chakrabarty (Duke University)

Observation Point Insertion using Deep Learning

Bonita Bhaskaran (NVIDIA Corporation)

Sanmitra Banerjee (NVIDIA Corporation)

Kaushik Narayanun (NVIDIA Corporation)

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Seyed Nima Mozaffari Mojaveri (NVIDIA Corporation)

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Technical Program: Wednesday, November 2

3:45 PM – 5:45 PM, Capri

14D Autonomous Systems and Machine Learning on Embedded Systems

Session Chair: Ibrahim (Abe) Elfadel (Khalifa University)

Session Co-Chair: Mimi Xie (UTSA)

Romanus: Robust Task Offloading in Modular Multi-Sensor Autonomous Driving Systems

Luke Chen (University of California Irvine)

Mohanad Odema (University of California Irvine)

Mohammad Al Faruque (University of California Irvine)

ModelMap: A Model-based Multi-domain Application Framework for Centralized Automotive Systems

Soham Sinha (Boston University)

Anam Farrukh (Boston University)

Richard West (Boston University)

INDENT: Incremental Online Decision Tree Training for Domain-Specific Systems-on-Chip

Anish Krishnakumar (University of Wisconsin-Madison)

Radu Marculescu (The University of Texas at Austin)

Umit Ogras (University of Wisconsin – Madison)

SGIRR: Sparse Graph Index Remapping for ReRAM Crossbar Operation Unit and Power Optimization

Cheng-Yuan Wang (National Taiwan University)

Yao-Wen Chang (National Taiwan University)

Yuan-Hao Chang (Academia Sinica)

Workshops: Thursday, November 3

Workshop on Open-Source EDA Technology (WOSET)

<https://woset-workshop.github.io/>

Virtually co-sponsored by ICCAD 2022 on November 3, 2022!

The WOSET workshop aims to galvanize the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open-source EDA flow. The workshop will feature presentations and posters that overview existing or under-development open-source tools, designs and technology libraries. A live demo session for tools in advanced state will be planned. The workshop will feature a panel on the present status and future challenges in open-source EDA, and how to coordinate efforts and ensure quality and interoperability across open-source tools.

Organizers:

Jose Renau (*UC Santa Cruz (Co-Chair)*)
Matthew Guthaus (*UC Santa Cruz (Co-Chair)*)
Jose Renau (*UC Santa Cruz*)
Matthew Venn (*YosysHQ & ChipFlow*)
Rajit Manohar (*Yale University*)
Scott Temple (*University of Utah*)
Jonathan Balkind (*UC Santa Barbara*)
Tobias Grosser (*University of Edinburgh*)
Jesse Cirimeli-Low (*UC Santa Cruz*)
Sakshi Garg (*UC Santa Cruz*)

Workshops: Thursday, November 3

Workshop on Zero Trust Hardware Architectures

<https://zerotrustworkshopiccad.github.io/>

In recent times, there has been a major push and urgency to adopt the zero-trust model for cybersecurity. The zero-trust model is based on the principle of “never trust, always verify” and is aimed at eliminating all implicit trust in a system. While adopting a zero-trust model for network security generally involves authenticating, authorizing and continuously validating the credentials of users in a network, these measures alone are not enough to create a true zero trust-based architecture. The underlying hardware needs to be trusted and secured as well. Thus, novel approaches for building zero trust architectures, from systems all the way down to silicon, is one of the big challenges for next generation hardware system design. Traditionally, research on establishing trust and security in hardware has primarily focused on the host and its associated memory subsystems. These include principles of trusted execution environments, silicon roots of trust, Trusted Platform Modules, encryption at rest etc. However, in modern system architectures such as edge/cloud computing, composable systems and chiplet based integrated circuits, the realm of trust needs to be extended beyond the host system and incorporate many hardware devices and IPs. In view of threats such as compromised supply chain integrity, counterfeit chips, hardware trojan implants, malicious firmware, malware, etc., it is important to establish trust in hardware components and to communicate trust between different components of a system. The different kinds of communication could range from that between different IPs inside a SoC, between a host and its attached peripherals, as well as between chiplets inside a multi-chip module. Trust also needs to be established and revoked in a dynamic manner, with the ability to handle large number of subcomponents in the design. Thus, a new set of protocols that can work to establish trust and security in these new types of system architectures has become necessary. While some of these protocols are being developed as industry and government standards, large-scale effort is required to bring them to adoption. It is equally important to develop open source and verifiable hardware designs that can bring security without compromising system parameters such as performance or functionality. The focus of this workshop will be on all aspects of security and trust required to create zero-trust hardware architectures for heterogeneous computing systems.

Organizers:

Sandhya Koteswara (*IBM Research*)

Mengmei Ye (*IBM Research*)

Hubertus Franke (*IBM Research*)

Workshops: Thursday, November 3

Workshop on Hardware and Algorithms for Learning On-a-chip (HALO)

<https://sites.google.com/rice.edu/iccad-halo-2022/home>

In recent years, machine/deep learning algorithms have unprecedentedly improved the accuracy in practical recognition and classification tasks, some even surpassing human-level accuracy. While significant progress has been made on accelerating the models for real-time inference on edge and mobile devices, the training of the models largely remains offline on the server side. State-of-the-art learning algorithms for deep neural networks (DNN) imposes significant challenges for hardware implementations in terms of computation, memory, and communication. This is especially true for edge devices and portable hardware applications, such as smartphones, machine translation devices, and smart wearable devices, where severe constraints exist in performance, power, and area.

There is a timely need to map the latest complex learning algorithms to custom hardware, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness. Exemplary efforts from industry and academia include many application-specific hardware designs (e.g., xPU, FPGA, ASIC, etc.). Recent progress in computational neurosciences and nanoelectronic technology, such as emerging memory devices, will further help shed light on future hardware-software platforms for learning on-a-chip. At the same time new learning algorithms need to be developed to fully explore the potential of the hardware architecture.

The overarching goal of this workshop is to explore the potential of on-chip machine learning, to reveal emerging algorithms and design needs, and to promote novel applications for learning. It aims to establish a forum to discuss the current practices, as well as future research needs in the aforementioned fields.

Organizers:

Yingyan (Celine) Lin (*Georgia Tech*)

Yanzhi Wang (*Northeastern University*)

Mandy Pant (*Intel*)

Workshops: Thursday, November 3

Top Picks in Hardware and Embedded Security

<https://www.ieee-hsttc.org/top-picks-2022/>

Top Picks recognizes the best of the best in hardware security, spanning the gamut from hardware to microarchitecture to embedded systems. Top Picks will be selected from hardware security papers that have appeared in leading conferences/journals, including but not limited to top security (e.g., IEEE S&P, NDSS, USENIX SEC), architecture (e.g., ISCA, ASPLOS), CAD (e.g., ICCAD, DAC, DATE), and hardware security (e.g., CHES) venues.

After submission, papers will undergo a down select, whereby “shortlisted” papers will be invited to the Top Picks workshop, co-located with ICCAD 2022. An author(s) of each shortlisted paper is required to present the paper in-person at the workshop. A subset of these will be selected as Top Picks. Select papers are then invited for submission to a special journal issue.

Organizers:

Ahmad-Reza Sadeghi (*Technical University of Darmstadt, Germany*)

Christopher Fletcher (*University of Illinois, Urbana Champaign, USA*)

Workshops: Thursday, November 3

4th Workshop on Accelerator Computer Aided Design (ACCAD 2022)

<https://sites.google.com/view/accad2022/home>

The ACCAD workshop provides a forum to present and discuss the current trends in computer-aided design in support of domain-specific accelerator chips, especially for artificial intelligence and machine learning applications. The workshop will be concerned with the VLSI methodology flow from high-level synthesis to physical verification and performance prediction, particularly in the way it gets impacted with the emerging design paradigms of domain-specific instruction sets, approximate computing, in-memory computing, and stochastic computing. Of particular interest to the workshop are the transformations that VLSI CAD has to undergo to adapt to the post-CMOS technologies when they are considered in the context of accelerator design. The workshop will include, but will not be limited to, the following topics:

- High-level synthesis of machine-learning accelerators.
- Design space exploration of domain-specific accelerators.
- Tools and methodologies for in-memory computing.
- Tools and methodologies for approximate computing.
- CAD for emerging accelerator technologies: ReRAM, MRAM, Photonics, etc.
- Tools and methodologies for the post-CNN era.
- Tools and methodologies for the testing and verification of accelerator chips.

Each year, the workshop will be devoted to four focus areas of accelerator CAD. Renowned speakers are invited to speak on each of the four areas. This edition of the workshop will feature both invited speakers and submitted presentations. Potential presenters should submit a two-page abstract describing the contents of their presentations. Abstracts will be reviewed and selected ones will be scheduled for oral presentations. Other selected abstracts may be featured in a poster session.

The four focus areas selected for this year are the following:

1. ML Compilers and their Quality of Results
2. AI Accelerator Virtualization for Cloud Computing
3. Acceleration on the Edge: ASIC or MCU?
4. AI Accelerators as a Cloud Service.

Organizers:

Ibrahim (Abe) Elfadel (*Khalifa University*)
Subhashish Mitra (*Stanford University*)

Workshops: Thursday, November 3

24th ACM/IEEE International Workshop on System-Level Interconnect Pathfinding (SLIP)

<http://www.sliponline.org/>

The 2022 ACM/IEEE International Workshop on **System-Level Interconnect Pathfinding (SLIP)** is the 24th edition of the Workshop. SLIP, co-located with ICCAD 2022, will bring together researchers and practitioners who have a shared interest in the challenges and futures of system-level interconnect, coming from wide-ranging backgrounds that span system, application, design and technology.

The technical goal of the workshop is to:

1. identify fundamental problems
2. foster new pathfinding of design, analysis, and optimization of system-level interconnects with emphasis on system-level interconnect modeling and pathfinding, DTCO-enhanced interconnect fabrics, memory and processor communication links, novel dataflow mapping for machine learning, 2.5/3D architectures, and new fabrics for the beyond-Moore era.

There are two special sessions this year:

1. Power distribution in advanced technology nodes
2. Tackling memory wall in many-core and AI systems

Organizers:

Mustafa Badaroglu (*Qualcomm*)
Shantanu Dutt (*Univ. of Illinois at Chicago*)
Pascal Vivet (*CEA*)
Ismail Bustany (*AMD*)
Rasit Topaloglu (*IBM*)
Seungwon Kim (*UCSD*)

SUSHI: Sustainable Hardware Security

<https://hardwaresec.42sec.de/>

The desire for digital sovereignty, recent global semiconductor shortages and geopolitical interests are driving forces behind various worldwide initiatives to strengthen semiconductor technology and manufacturing on a national and regional basis. In this context, hardware security will play a vital role since hardware is at the heart of all computing systems, and insecure hardware will put critical systems and consequently, our society at risk.

However, in recent years, we are observing the discovery of a growing number of hardware design and implementation vulnerabilities that could be exploited by unprivileged software, leading to potential exposure of sensitive data or compromise of whole computing systems. This new attack paradigm casts a long shadow on decades of research on system security and disrupts the traditional threat models that have mainly focused on software-only vulnerabilities and often assume that the underlying hardware is behaving correctly and is trustworthy. Unfortunately, existing solutions are often ad-hoc, limited, inefficient, and address only specific problems.

The main goal of this workshop is to bring together international researchers and experts from academia, industry, and government to exchange knowledge and explore new ideas and research directions for tackling the challenges related but not limited to security-by-design for hardware, scalable assurance methodologies for hardware security and resilience, and security-aware electronic design automation that pave the way for establishing sustainable security for computing platforms.

Organizers:

Adam Cron (*Synopsys*)

Jason Fung (*Intel*)

Farianz Koushanfar (*UC San Diego*)

Jeyavijayan Rajendran (*Texas A&M*)

Ahmad-Reza Sadeghi (*TU Darmstadt*)

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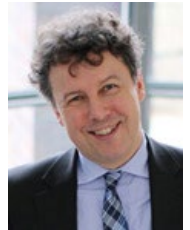
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ACM/SIGDA, Special Interest Group on Design Automation) provides a broad array of resources to our members, to students, professors, industry professionals and, to the EDA field in general. SIGDA sponsors various events to promote interaction among the community to share the latest technical and professional advances. It also serves as a forum to support events that nurture new ideas and infuse vitality into new emerging trends in the field.

SIGDA has a long history of supporting conferences and the EDA profession including ICCAD, DAC, DATE, and ASP-DAC, plus around 15 focused symposia and workshops. SIGDA supports various events such as - the Univ. Research Demonstration that helps to foster interactions between students and industry; Design Automation Summer School that exposes students to trending topics; Young Faculty Workshops; Ph.D. Forums in conjunction with major conferences, design contests such as CAD Athlon. SIGDA funds various scholarships and recognizes outstanding research publications. Awards recognize significant contributions at all stages of the professional career from student awards to the Pioneer Award for Lifetime achievement. SIGDA has launched new programs such as SIGDA Live, a series of monthly webinars on topics of general interest to the SIGDA community and a more global E-Newsletter with a newly formed editorial board. SIGDA also supports local chapters that help with professional networking. SIGDA also administers Student Research Competition on behalf of ACM.

SIGDA pioneered electronic publishing of EDA literature, beginning with the DA Library in 1989. SIGDA also provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems). Major benefits provided to SIGDA members include free access to all SIGDA sponsored publications in the ACM Digital Library, and reduced registration rates for SIGDA sponsored events.

For further information on SIGDA's programs and resources, see <http://www.sigda.org>. Please join us in building a more vibrant community and volunteer for SIGDA.

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IEEE is the world's largest professional association dedicated to advancing technological innovation and excellence for the benefit of humanity. IEEE and its members inspire a global community through IEEE's highly cited publications, conferences, technology standards, and professional and educational activities.



The IEEE Council on Electronic Design Automation (CEDA) was established to foster design automation of electronic circuits and systems at all levels. The Council's field of interest spans the theory, implementation, and use of EDA/CAD tools to design integrated electronic circuits and systems. This includes tools that automate all levels of the design, analysis, and verification of hardware and embedded software up to and including complete working systems.

CEDA enables the exchange of technical information by means of publications, conferences, workshops, and volunteer activities.

As an organizational unit (OU) of IEEE, CEDA has seven member societies, namely: Antennas and Propagation, Circuits and Systems, Computer, Electron Devices, Electronics Packaging, Microwave Theory & Techniques, and Solid-State Circuits Societies.

For more information on CEDA, visit: <http://www.ieee-ceda.org>.



The IEEE Circuits and Systems Society's field of interest spans the theory, analysis, design (computer aided design), and practical implementation of circuits, and the application of circuit theoretic techniques to systems and to signal processing. The coverage of this field includes the spectrum of activities from, and including, basic scientific theory to industrial applications.

The IEEE Circuits and Systems Society (CASS) believes that the Grand Engineering Challenges of the 21st century can only be addressed in an inter-disciplinary and cross-disciplinary manner. The Society's unique and profound expertise in Circuits, Systems, Signals, Modeling, Analysis, and Design can have a decisive impact on important issues such as Sustainable Energy, Bio-Health, Green Information Technology, Nano-Technology, and Scalable Information Technology Systems. Our mission is to foster CASS members across disciplines to address humanity's grand challenges by conceiving and pioneering solutions to fundamental and applied problems in circuits and systems.



The IEEE Electron Devices Society (EDS) is involved in the advancement of electronics and electrical engineering through research, development, design, manufacture, materials, and applications of electron devices. EDS is concerned with technical, educational, scientific publication and meeting activities which provide benefits to members while contributing towards the progress of this field. <http://www.eds.ieee.org>.

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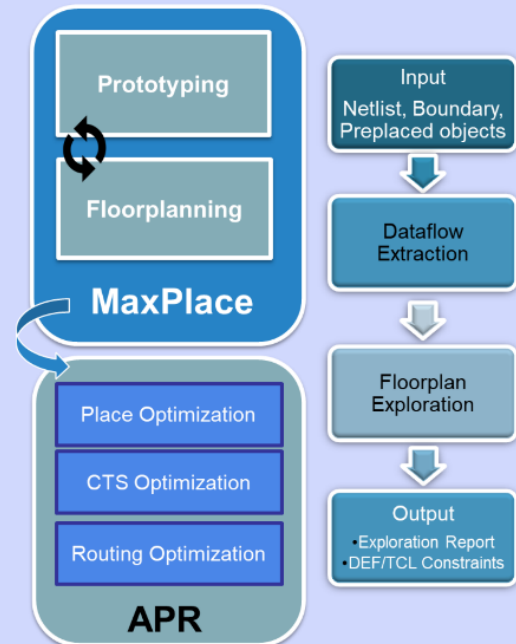
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CALL FOR PAPERS

Original technical submissions on, but not limited to, the following topics are invited:

1) SYSTEM-LEVEL CAD

1.1 System Design

- » System-level specification, modeling, simulation, design flows
- » System-level issues for 3D integration
- » System-level design case studies and applications
- » HW/SW co-design, co-simulation, co-optimization, and co-exploration, platforms for emulation and rapid prototyping
- » Micro-architectural transformation
- » Multi-/many-core processor, GPU and heterogeneous SoC
- » Memory and storage architecture and system synthesis
- » System communication architecture, Network-on-chip design
- » Modeling, simulation, high-level synthesis, power/performance analysis, programming of heterogeneous computing platforms
- » Application driven system design for big data
- » Analysis and optimization of data centers

1.2 Embedded, Cyber-Physical (CPS), IoT Systems and Software

- » AI and machine learning for embedded systems
- » HW/SW co-design for embedded systems
- » Compute, memory, storage, interconnect for embedded systems
- » Domain-specific accelerators
- » Energy/power management and energy harvesting
- » Real-time software and systems
- » Middleware, virtual machines, and runtime support
- » Dependable, safe, secure, trustworthy embedded systems
- » Embedded software: compilation, optimization, testing
- » CAD for IoT, edge and fog computing
- » Modeling, analysis, verification of CPS systems
- » Green computing (smart grid, energy, solar panels, etc.)
- » CAD for application domains including wearables, health care, autonomous systems, smart cities

1.3 Tools and Design Methods with and for Artificial Intelligence (AI)

- » Compilers for deep neural networks
- » Design method for learning on a chip
- » Deep neural network for EDA
- » Tools and design methodologies for edge AI and TinyML
- » Performance analysis and modeling for AI accelerators
- » Reliability analysis for neural network designs

1.4 Hardware Systems and Architectures for Artificial Intelligence (AI)

- » Hardware and architecture for neural networks
- » System-level design for (deep) neural computing

- » Neural network acceleration including GPU and ASICs
- » Safe and secure machine learning
- » Hardware accelerators for Artificial Intelligence (e.g., neural network, graph processing)
- » Edge AI and TinyML architecture designs
- » New systems and architectures for neural networks, such as optical neural networks, chiplets

1.5 Reconfigurable Computing

- » Novel reconfigurable architectures (FPGA, CGRA, etc.)
- » Neural network acceleration on reconfigurable accelerators
- » High-level synthesis on reconfigurable architectures
- » Compilers for reconfigurable architectures
- » Reconfigurable fabric security
- » HW/SW prototyping and emulation on FPGAs
- » Post-synthesis optimization for FPGAs
- » FPGA-based prototyping for analog, mixed-signal, RF systems

1.6 Algorithms and Tools for Hardware Security

- » New physical attack vectors or methods for ASICs
- » Split Manufacturing for security
- » Supply chain security and anti-counterfeiting
- » Artificial Intelligence for attack prevention systems
- » Privacy-preserving computation

1.7 Architecture and Systems for Hardware Security

- » Hardware Trojans, side-channel attacks, fault attacks and countermeasures
- » Nano electronic security
- » Hardware-based security (CAD for PUF's, RNG, AES etc.)
- » Design and CAD for security
- » Trusted execution environments
- » Cloud Computing data security
- » Sensor network security

1.8 Low Power and Approximate Computing

- » Power and thermal estimation, analysis, optimization, and management techniques for hardware and software systems
- » Energy- and thermal-aware application mapping and scheduling
- » Energy- and thermal-aware architectures, algorithms
- » Energy- and thermal-aware dark silicon system design
- » Hardware techniques for approximate/stochastic computing

2) SYNTHESIS, VERIFICATION, PHYSICAL DESIGN, ANALYSIS, SIMULATION, AND MODELING

2.1 High-Level, Behavioral, and Logic Synthesis and Optimization

- » High-level/Behavioral/Logic synthesis
- » Technology-independent optimization and technology mapping
- » Functional and logic timing ECO (engineering change order)
- » Resource scheduling, allocation, and synthesis
- » Interaction between logic synthesis and physical design

2.2 Testing, Validation, Simulation, and Verification

- » High-level/Behavioral/Logic modeling, validation, simulation
- » Formal, semi-formal, and assertion-based verification
- » Equivalence and property checking
- » Emulation and hardware simulation/acceleration
- » Post-silicon validation and debug
- » Digital fault modeling and simulation
- » Delay, current-based, low-power test
- » ATPG, BIST, DFT, and compression
- » Memory test and repair
- » Core, board, system, and 3D IC test

2.3 Cell-Library Design, Partitioning, Floorplanning, Placement

- » Cell-library design and optimization
- » Transistor and gate sizing
- » High-level physical design and synthesis
- » Estimation and hierarchy management
- » 2D and 3D partitioning, floorplanning, and placement
- » Post-placement optimization
- » Buffer insertion and interconnect planning

2.4 Clock Network Synthesis, Routing, and Post-Layout Optimization and Verification

- » 2D and 3D clock network synthesis
- » 2D and 3D global and detailed routing
- » Package-/Board-level
- » Chip-package-board co-design
- » Post-layout/-silicon optimization
- » Layout and routing issues for optical interconnects

2.5 Design for Manufacturability and Design for Reliability

- » Process technology characterization, extraction, and modeling
- » CAD for design/manufacturing interfaces
- » CAD for reticle enhancement and lithography-related design
- » Variability analysis and statistical design and optimization
- » Yield estimation and design for yield
- » Physical verification and design rule checking
- » Machine learning for smart manufacturing and process control
- » Analysis and optimization for device-level reliability issues
- » Analysis optimization for interconnect reliability issues
- » Reliability issues related to soft errors
- » Design for resilience and robustness

2.6 Timing, Power and Signal Integrity Analysis and Optimization

- » Deterministic and statistical static timing analysis, optimization
- » Power and leakage analysis and optimization
- » Circuit and interconnect-level low power design issues
- » Power/ground network analysis and synthesis
- » Signal integrity analysis and optimization

2.7 CAD for Analog/Mixed-Signal/RF and Multi-Domain Modeling

- » Analog, mixed-signal, and RF noise modeling, simulation, test
- » Electromagnetic simulation and optimization
- » Device, interconnect and circuit extraction and simulation
- » Behavior modeling of devices and interconnect
- » Package modeling and analysis

3) CAD FOR EMERGING TECHNOLOGIES, PARADIGMS

3.1 Bio-inspired and Neuromorphic Computing

- » Hardware for neuromorphic computing
- » Event or spike-based hardware systems
- » CAD for microfluidics
- » CAD for biological computing systems
- » CAD for synthetic biology
- » CAD for bio-electronic devices, bio-sensors, MEMS

3.2 Nanoscale and Post-CMOS Systems

- » New device structures and process technologies
- » New memory technologies (flash, PCM, STT-RAM, memristor)

- » Nanotechnologies, nanowires, nanotubes, graphene, etc.
- » CAD for mixed-domain (semiconductor, nanoelectronic, MEMS, and electro-optical) devices, circuits, and systems
- » CAD for nanophotonics and optical devices/communication
- » CAD for field-coupled nanotechnologies
- » Device, interconnect and circuit extraction and simulation
- » Behavior modeling of devices and interconnect

3.3 New Computing Paradigm

- » Non-von Neumann architectures
- » Quantum computing

SUBMISSION DETAILS

Paper submissions must be made through the online submission system at the [ICCAD website](#).

Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage. Research papers with open-source software are highly encouraged where the software will be made publicly available (via GitHub or similar) with the camera-ready version if the paper has been accepted. For protecting the authors' identities in the double-blind review process, please do not include direct link to the non-anonymized software in the submitted paper but indicate the open-source contribution on a textual basis only. Authors wanting to share GitHub repositories may want to look into using <https://anonymous.4open.science> which is an open-source tool that helps you to quickly Double-blind your repository.

Authors are asked to submit their work in two stages. In stage one (abstract submission), a title, abstract, and a list of all co-authors must be submitted via the ICCAD web submission site. In stage two (paper submission), the paper itself is submitted whereby the submitted abstract of stage one can still be modified. Authors are responsible for [declaring COIs](#), ensuring that their paper submission meets all guidelines, and that the PDF is readable.

DEADLINE FOR ABSTRACT AND PAPER SUBMISSIONS

The abstract submission deadline is Monday, May 15, 2023 at 23:59 AOE. No abstract submissions will be possible after this deadline.

The paper submission deadline is Monday, May 22, 2023 at 23:59 AOE.

We always have several authors contact the ICCAD office asking for a deadline extension. Due to the limited review cycle, NO extensions will be granted for ANY reason.

REGULAR PAPER SUBMISSIONS

- » All papers must be in PDF format only, with savable text and embedded fonts in included (vector) graphics.
- » Each paper must be no more than 8 pages (including the abstract, figures and tables), double-columned, 9pt or 10pt font. One page of references is allowed, which does not count towards this 8-page limitation.
- » Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the author(s) own published works or affiliations should be made in the third person.
- » Submissions not adhering to these rules, or determined to be previously published or simultaneously submitted to another conference, or journal, will be summarily rejected. Internal memoranda with full content not publicly available, and with author names not divulged, may be submitted.

IMPORTANT: Final camera-ready versions must be identical to the submitted papers with the following exceptions; inclusion of author names/affiliation, correction of identified errors, addressing reviewer demanded changes. No other modifications of any kind are allowed including modification of title, change of the author list, reformatting, restyling, rephrasing, removing figures/results/text, etc. The TPC Chairs reserve the right to finally reject any manuscripts not adhering to these rules.

TEMPLATES

Paper templates are available at the ICCAD website and authors are recommended to format their papers based on the IEEE template.

NOTIFICATION OF ACCEPTANCE

Authors will be notified of acceptance on or before, July 21, 2023. Final paper guidelines will be sent at that time.

PROCEEDINGS

The deadline for final camera-ready papers is August 14, 2023. Accepted regular papers are allowed six pages plus one page of references in the conference proceedings free of charge. Each additional page (except references) beyond six pages is subject to the page charge at \$150.00 per page up to the eight-page plus one page of references. ACM will hold the copyright for ICCAD 2023 proceedings. Authors of accepted papers must sign an ACM copyright release form for their paper.

CONFERENCE REGISTRATION

At least one author per accepted regular paper or poster must be registered by August 18, 2023 in the conference. Failure to register will result in your paper being removed from the conference proceedings. In case of a regular paper, ACM reserves the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library) if the paper is not presented at the conference.

ACM/IEEE WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

Two papers from this year's ICCAD conference (one from front-end and one from back-end) will receive this prestigious award. The winners will be chosen from nominated papers after a thorough and competitive process by the area-specific selection committees and announced at the conference opening session.

ICCAD TEN-YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

One paper from the 2013 and 2014 editions of ICCAD will be selected for the 10-year retrospective most influential paper award as evidenced by impact on the research community as reflected in citations, on the vendor community via its use in an industrial setting, or on new research venues as initiated by the paper during the past decade. Nominations from the community are welcome and can be sent to Robert Wile, Technical Program Vice Chair at robert.wile@tum.de.

CALL FOR PROPOSALS

Call for Workshop, Tutorial, Special Session, Panel and Keynote Proposals are all due on Monday May 22, 2023.

WORKSHOP PROPOSALS

ICCAD provides a vibrant and supportive environment for small-to-medium-sized affiliated workshops. Typical workshops are one-day events on the Thursday of ICCAD. All workshop proposals should be submitted through the ICCAD website.

TUTORIAL PROPOSALS

All ICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and a good audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of two session blocks of 1.5-2 hours each) may be considered. Tutorial proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. Proposals should focus on the state-of-the-art in a specific area of broad interest amongst ICCAD attendees. All tutorial proposals should be submitted through the ICCAD website and questions can be addressed to Deming Chen, Tutorial and Special Sessions Chair, at dchen@illinois.edu. Please read the proposal guidelines at [ICCAD website](#).

SPECIAL SESSION PROPOSALS

Special Sessions typically run 1.5-2 hours. Special session proposals should focus on in-depth treatment on a topic of timely interest to the ICCAD audience. Special session proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. All special session proposals should be submitted through the ICCAD website and questions can be addressed to Deming Chen, Tutorial and Special Sessions Chair, at dchen@illinois.edu. Please read the proposal guidelines at [ICCAD website](#).

IF YOU NEED ASSISTANCE, PLEASE CONTACT THE APPROPRIATE COMMITTEE MEMBERS

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Program Chair: Jinjun Xiong, jinjun@buffalo.edu