



CONFERENCE PROGRAM

NOVEMBER 7-10, 2016 • AUSTIN, TX • ICCAD.COM



In cooperation with:
IEEE Electron Devices Society



- WELCOME TO THE 35TH ICCAD -



Welcome to the 35th edition of the International Conference on Computer-Aided Design! For the second year in a row, ICCAD is held in Austin, Texas. Jointly sponsored by IEEE and ACM, ICCAD is the premier forum to explore emerging technology challenges, present cutting-edge R&D solutions, record theoretical and empirical advances, and identify future roadmaps for design automation and other system-on-chip research areas. The members of the executive committee, the technical program committee, and numerous volunteers have spent the past eleven months to prepare an exciting program for you.

At the core of the conference program is the technical program, which spans 27 regular sessions. Thanks to the strong support from the community, we continue to see a solid growth in the paper submissions: after a remarkable 25% increase of papers in 2015, this year we observed another 7% of growth in submissions worldwide. The total 409 submissions, organized into 17 tracks, were reviewed by 114 outstanding TPC members, with a balanced representation from worldwide experts in both academia and industry. Our rigorous double-blind review process culminated with a full-day in-person meeting in June, where 97 regular papers were selected to be included in the proceedings. This marks another excellent year of submissions and a competitive selection process of a 24% acceptance rate.

In addition to the 27 regular sessions, this year's program also features nine special sessions, three embedded tutorials, and one embedded panel. The scope of the presentations spans all aspects of contemporary topics in design automation, system-level design, as well as advanced topics on hardware security, cyber-physical systems, and hardware for machine learning. After last year's experiment, we are happy to announce that ICCAD program is going mobile: the organizing committee is placing more program content into our mobile app. It includes many new features to help the attendees achieve better conference experience, and to have more networking opportunities.

Following a long tradition, ICCAD continues to be the home of strong student-oriented activities: the SIGDA CADathlon, the ACM Student Research Competition, and the ICCAD CAD Contest. This year marks the fifteenth anniversary of the SIGDA CADathlon competition which gathers the brightest minds in design automation and SoC design for a full day of intensive speed coding. The winners will be announced at the Opening Session on Monday morning. This year also marks the fifth edition of the ICCAD CAD Contest, which is one of the largest CAD contests in the world. This year the CAD Contest has reached another record, 135 participating teams from eleven countries/regions. Please make sure to attend the CAD Contest Special Session on Monday afternoon to learn the winners and the details of the contest benchmarks.

We are fortunate to host several distinguished keynote speakers: the Monday morning keynote on silicon photonics will be given by Professor Michal Lipson from Columbia University, a 2010 MacArthur Fellow. On Tuesday, Dr. Maarten Sierhuis of the Nissan Research Center will present the IEEE CEDA Luncheon Distinguished Lecture on socially acceptable AI-based city driving. Finally Professor Peter Stone, the David Bruton, Jr. Centennial Professor of Computer Science at the University of Texas at Austin, will present the Wednesday keynote on learning and multiagent reasoning for autonomous robots. We hope these keynotes, together with the rest of the conference, will make ICCAD an ultimate destination for all researchers and practitioners.

We are grateful to our ICCAD 2016 sponsors and numerous supporters for making this year's conference another successful event.

Enjoy ICCAD! Enjoy Austin!

A handwritten signature in black ink that reads "Frank Liu".

ICCAD 2016 GENERAL CHAIR

Frank Liu
IBM Research Austin

- TABLE OF CONTENTS -

Welcome Message	2
General Information	4
Best Paper Candidates & Committees	6
CADathlon at ICCAD	7
Monday Schedule	8
Opening Session & Award Presentations	10
Monday Keynote Address	11
Monday Session Details	12
ACM Student Research Competition Poster Session	15
ACM Student Research Competition Technical Presentations	23
Tuesday Schedule	24
Tuesday Session Details	26
Tuesday Invited Keynote Luncheon	32
ACM/SIGDA Membership Meeting	41
Wednesday Schedule	42
Wednesday Keynote Address	44
Wednesday Session Details	45
Thursday Schedule	56
Thursday Workshop Details	57
Executive Committee	61
Technical Program Committee	62
Conference Sponsors	64

Registration Hours & Location

Room: Prefunction Central

Monday, November 7	7:00am - 6:00pm
Tuesday, November 8	7:30am - 6:00pm
Wednesday, November 9	7:30am - 6:00pm
Thursday, November 10	7:00am - 4:00pm

ICCAD 2016 Mobile App

Review the program, save sessions to your personalized conference schedule, read speakers abstracts, and connect with other attendees using the ICCAD 2016 mobile app provided by Whova, available for download today. Download Whova and search for **ICCAD 2016**.



Shuttle Information

ICCAD attendees can catch the shuttle to downtown Austin on Tuesday night from 6:00pm - 12:00am (Midnight). Service runs between the DoubleTree Hotel and the Driskill Hotel downtown.

Locations and Schedule:

Departing from the DoubleTree Hotel (In front of the hotel under the Porte Cochere):
6:00pm, 7:00pm, 8:00pm, 9:00pm, 10:00pm, 11:00pm

Departing from the Driskill Hotel downtown on the half hour:
6:30pm, 7:30pm, 8:30pm, 9:30pm, 10:30pm, 11:30pm

Proceedings

ICCAD Conference Papers will be delivered electronically online via a username and password.

To access: <http://proceedings.iccad.com>

Username = Email address

Password = Registration ID (on your badge)

Please refer to your registration receipt to access the files you are eligible to view.

Parking Information

Attendees receive complimentary day use self-parking and \$5.00/day overnight self-parking at the DoubleTree by Hilton Austin.

For Speakers & Presenters

SPEAKERS' BREAKFAST

Please attend the day of your presentation!

Room: Phoenix Central

Monday, November 7	8:00 - 8:45am
Tuesday, November 8	7:45 - 8:30am
Wednesday, November 9	8:00 - 8:45am

NEED PRACTICE?

The DeWitt and Fourth Floor Capital rooms are available and are set up with a computer, LCD projector and screen to view your slides before your session.

Room: DeWitt

Monday, November 7	7:00am - 6:00pm
Tuesday, November 8	7:00am - 6:00pm

Room: Fourth Floor Capital

Wednesday, November 9	7:00 - 11:00am
-----------------------	----------------

ICCAD Social Media



Connect with ICCAD through Twitter @ICCAD. ICCAD will be tweeting hourly updates and conference highlights!



Find ICCAD on LinkedIn and keep up to date with the latest news and insights.

Conference Management



Our mission is to facilitate networking, education and marketing with efficiency and precision in order to maximize customer experiences, and client profitability and recognition. We accomplish this by having a committed staff of trade show production organizers with the training, technology tools, processes and experience to offer the best service in the industry.

Visit mpassociates.com for more information.

- BEST PAPER CANDIDATES & AWARD COMMITTEES -

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

MONDAY, NOVEMBER 7

1A.1 Scope - Quality Retaining Display Rendering Workload Scaling based on User-Smartphone Distance

Kent Nixon, Xiang Chen, Yiran Chen - *Univ. of Pittsburgh*

2C.1 Improved Flop Tray-Based Design Implementation for Power Reduction

Andrew B. Kahng, Jiajia Li, Lutong Wang - *Univ. of California at San Diego*

TUESDAY, NOVEMBER 8

4A.1 Malicious LUT: A Stealthy FPGA Trojan Injected and Triggered by the Design Flow

Christian Krieg, Clifford Wolf, Axel Jantsch - *Technische Univ. Wien*

WEDNESDAY, NOVEMBER 9

9A.1 Fast Physics-Based Electromigration Checking for On-Die Power Grids

Sandeep Chatterjee - *Univ. of Toronto*

Valeriy Sukharev - *Mentor Graphics Corp.*

Farid N. Najm - *Univ. of Toronto*

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee

Vijaykrishnan Narayanan (Chair) - *Pennsylvania State Univ.*

Rolf Drechsler - *Univ. of Bremen & DFKI GmbH*

Azadeh Davoodi - *Univ. of Wisconsin-Madison*

Yu Wang - *Tsinghua Univ.*

Ten-Year Retrospective Most Influential Paper Award Selection Committee

Martin Wong (Chair) - *Univ. of Illinois at Urbana-Champaign*

Kaustav Banerjee - *Univ. of California, Santa Barbara*

Ramesh Karri - *New York Univ.*

Jason Cong - *Univ. of California, Los Angeles*

Tulika Mitra - *National Univ. of Singapore*

- ACM SIGDA CADATHLON 2016 AT ICCAD -

ACM SIGDA CADathlon 2016 at ICCAD

Sunday, November 6, 8:00am - 5:00pm | Phoenix South

The CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork.

In its fifteenth year as the "Olympic games of EDA," the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field.

The contest is open to two-person teams of graduate students specializing in CAD and currently full-time enrolled in a Ph.D. granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Travel grants are provided to qualifying students.

The CADathlon competition consists of six problems in the following areas:

- (1) Circuit analysis
- (2) Physical design
- (3) Logic and behavioral synthesis
- (4) System design and analysis
- (5) Functional verification
- (6) Future technologies (Bio-EDA, Security, etc.)

More specific information about the problems and relevant research papers will be released on the Internet one week prior to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given. The team that earns the highest score is declared the winner. In addition to handsome trophies, the first and second place teams will receive cash award.

Contest winners will be announced at the ICCAD Opening Session on Monday morning and celebrated at the ACM/SIGDA Dinner and Member Meeting on Tuesday evening.

The CADathlon competition is sponsored by ACM/SIGDA and several Computer and EDA companies. For detailed contest information and sample problems from last year's competition, please visit the ACM/SIGDA website at <http://www.sigda.org/programs/cadathlon>

ORGANIZING COMMITTEE:

Chair: Myung-Chul Kim (mckima@us.ibm.com)

Vice Chair: Jingtong Hu (jthu@okstate.edu)

Vice Chair: Iris Hui-ru Jiang (hrjiang@faculty.nctu.edu.tw)

Sponsored by:



Association for
Computing Machinery



- MONDAY SCHEDULE -

8:45 - 9:15am

Opening Session & Awards

Room: Phoenix South

9:15 - 10:00am

Keynote: Manipulating Light on Chip

Michal Lipson - Columbia Univ. | Room: Phoenix South

10:00 - 10:30am

Coffee Break

Room: Prefunction Foyer

10:30am - 12:00pm

Session 1A: Innovative System Design Technologies

Room: Phoenix South

Session 1B: Topics in Low-level Logic Synthesis

Room: Austin

Session 1C: The Devil is in the Details: Incremental Placement Techniques

Room: Robertson

Special Session 1D: Emerging Technologies and Hardware Security: Prospects and Challenges

Room: Phoenix North

11:30am - 1:30pm

ACM Student Research Competition Poster Session

Room: Dover's

Sponsored by:



Association for
Computing Machinery



Microsoft

Research

12:15pm - 1:15pm

Lunch

Room: Phoenix Central

1:30 - 3:30pm

Session 2A: Accelerators and Design Methodologies for Brain-inspired Computing

Room: Phoenix South

Session 2B: Advanced Simulation Techniques and Optimization of Analog/RF Circuits

Room: Austin

Session 2C: Routing and Clocking

Room: Robertson

Special Session 2D: Future Value in ICs: Who Will Deliver It, and How

Room: Phoenix North

- MONDAY SCHEDULE -

3:30 - 4:00pm

Coffee Break

Room: Prefunction Foyer

4:00 - 5:30pm

Session 3A: Camouflaging and Obfuscation

Room: Phoenix South

Session 3B: Optimizing Memory and Flip-flops

Room: Austin

4:00 - 6:00pm

Special Session 3C: Design Automation for Next-Generation Automotive Systems

Room: Robertson

Special Session 3D: 2016 CAD Contest

Room: Austin

Sponsored by:



5:30 - 6:15pm

Networking Reception

Room: Phoenix Foyer

6:00 - 8:00pm

ACM Student Research Competition Technical Presentations

Room: Phoenix South

Sponsored by:



6:15 - 8:00pm

Cadence Sponsored Dinner and Presentation

Room: Phoenix Central

Sponsored by:



Opening Session and Award Presentations

Time: 8:45am | Room: Phoenix South

Kick off the conference with opening remarks from the ICCAD Executive Committee members and hear the highlights of the conference. The IEEE/ACM William J. McCalla ICCAD Best Paper award will be announced along with other award presentations from IEEE and ACM.

IEEE/ACM WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

Front-End Award:

4A.1 Malicious LUT: A Stealthy FPGA Trojan Injected and Triggered by the Design Flow

Christian Krieg, Clifford Wolf, Axel Jantsch - *Technische Univ. Wien*

Back-End Award:

9A.1 Fast Physics-Based Electromigration Checking for On-Die Power Grids

Sandeep Chatterjee - *Univ. of Toronto*

Valeriy Sukharev - *Mentor Graphics Corp.*

Farid N. Najm - *Univ. of Toronto*

TEN YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design over the ten years since its original appearance at ICCAD.

2006 Paper Titled: An Analytical Model for Negative Bias Temperature Instability

Sanjay V. Kumar, Chris H. Kim, Sachin S. Sapatnekar - *Univ. of Minnesota*

ICCAD 2006, pp. 493 – 496

2016 ACM/SIGDA PIONEER AWARD

C. L. (David) Liu - *National Tsing Hua Univ.*

Mei Yi-Chi Honorary Chair Professor of Computer Science

IEEE CEDA OUTSTANDING SERVICE AWARD

Diana Marculescu - *Carnegie Mellon Univ.*

For outstanding service to the EDA community as ICCAD General Chair in 2015.

IEEE CEDA ERNEST S. KUH EARLY CAREER AWARD

Mohammad Abdullah Al Faruque - *University of California, Irvine*

For contributions to energy efficient design of reliable embedded and cyber-physical systems.

ACM/SIGDA CADATHALON

Introduction of the 2016 winners.



Keynote: Manipulating Light on Chip

Time: 9:15am - 10:00am | Room: Phoenix South

Speaker:

Michal Lipson - *Columbia Univ.*

Photonics on chip could enable a platform for monolithic integration of optics and microelectronics for applications of optical interconnects in which high data streams are required in a small footprint. This approach could alleviate some of the current bottlenecks in traditional microelectronics. In this talk I will review the challenges and achievement in the field of Silicon Nanophotonics and present our recent results. Using highly confined photonic structures, much smaller than the wavelength of light, we have demonstrated ultra-compact passive and active silicon photonic components that enhance the electro-optical, mechanical and non-linear properties of Silicon. Based on the ability to dynamically modulate light on the same time scale as the time of flight we have demonstrated novel GHz structures for a variety of applications.

Biography:

Professor Michal Lipson joined the Electrical Engineering faculty at Columbia University in July 2015. She completed her B.S., M.S., and Ph.D. degrees in Physics at the Technion in 1998 followed by a Postdoctoral position at MIT in the Materials Science Department till 2001. In 2001 she joined the School of Electrical and Computer Engineering at Cornell University. She was named Cornell Given Foundation Professor of Engineering in 2013. Lipson was one of the main pioneers in the field of silicon photonics and is the inventor of several of the critical building blocks in the field including the GHz silicon modulator. She holds over 20 patents and is the author of over 200 technical papers. Prof. Lipson held several leadership positions in the scientific community including, IEEE Photonics society board of directors member, co-organized numerous symposia and sessions in OSA conferences. She chaired and served on numerous committees including the Micro and Nanophotonics Subcommittee of CLEO, which she chaired 2006-2009. She has served as a topical editor (integrated photonics) for Optics Letters and served as a guest editor for IEEE Journal of Selected Topics of Electronics. She is currently serving on the board of directors for two international photonics centers, two start up companies and on the Rice ECE Advancement Committee. She is a co-founder of PicoLuz, a company specializing in nonlinear silicon photonic components. Professor Lipson's honors and awards include the MacArthur Fellow, Blavatnik Award, IBM Faculty Award, and the NSF Early Career Award. She is a fellow of OSA and IEEE. In 2014, and in 2015 she was named by Thomson Reuters as a top 1% highly cited researcher in the field of Physics.

1A - Innovative System Design Technologies

Time: 10:30am - 12:00pm | Room: Phoenix South

Moderator:

Umit Y. Ogras - *Arizona State Univ.*

This session introduces diverse innovative methods for System Design. This includes one paper on exploiting human visual perception's dependency on distance to adjust the resolution and framerate of mobile GPUs in smartphones, another paper describing a novel circuit-level simulator for emerging non-volatile memories to make informed system design decisions, and a final paper on a novel wavelength assignment method for optical NoCs.

***1A.1 Scope - Quality Retaining Display Rendering Workload Scaling based on User-Smartphone Distance**

Kent Nixon, Xiang Chen, Yiran Chen - *Univ. of Pittsburgh*

1A.2 NVsim-CAM: A Circuit-Level Simulator for Emerging Nonvolatile Memory based Content-Addressable Memory

Shuangchen Li, Liu Liu, Peng Gu - *Univ. of California, Santa Barbara*

Cong Xu - *Hewlett-Packard Labs.*

Yuan Xie - *Univ. of California, Santa Barbara*

1A.3 Design Technology for Fault-Free and Maximally-Parallel Wavelength-Routed Optical Networks-on-Chip

Andrea Peano, Luca Ramini, Marco Gavanelli, Maddalena Nonato, Davide Bertozzi
- *Univ. di Ferrara*

1B - Topics in Low-level Logic Synthesis

Time: 10:30am - 12:00pm | Room: Austin

Moderator:

Jacob Abraham - *Univ. of Texas at Austin*

This session presents three papers on low-level logic synthesis techniques. The first paper presents a technique for lexicographical enumeration of All-SAT solutions. The second paper offers a new technique for linear composition of threshold logic gates with equivalence checking. The final paper explores flash memory for digital circuit realization.

1B.1 Fast Generation of Lexicographic Satisfiable Assignments: Enabling Canonicity in SAT-Based Applications

Ana Petkovska - *École Polytechnique Fédérale de Lausanne*

Alan Mishchenko - *Univ. of California, Berkeley*

Mathias Soeken, Giovanni De Micheli - *École Polytechnique Fédérale de Lausanne*

Robert Brayton - *Univ. of California, Berkeley*

Paolo Ienne - *École Polytechnique Fédérale de Lausanne*

1B.2 Analytic Approaches to the Collapse Operation and Equivalence Verification of Threshold Logic Circuits

Nian-Ze Lee, Hao-Yuan Kuo, Yi-Hsiang Lai, Jie-Hong Roland Jiang - *National Taiwan Univ.*

1B.3 A Flash-based Digital Circuit Design Flow

Monther Abusultan, **Sunil P. Khatri** - *Texas A&M Univ.*

1C - The Devil is in the Details: Incremental Placement Techniques

Time: 10:30am - 12:00pm | Room: Robertson

Moderator:

Myung-Chul Kim - *IBM Corp.*

This session discusses new advances in detailed placement. The first paper proposes a technique to handle cells with multiple-row heights using a more comprehensive handling of complex constraints. The second paper covers an incremental path smoothing procedure coupled with timing optimization techniques. The third paper describes a parallel dynamic programming approach for FPGA detailed placement.

1C.1 **MrDP: Multiple-row Detailed Placement of Heterogeneous-sized Cells for Advanced Nodes**

Yibo Lin - *Univ. of Texas at Austin*

Bei Yu - *Chinese Univ. of Hong Kong*

Xiaoqing Xu - *Univ. of Texas at Austin*

Jih-Rong Gao, Natarajan Viswanathan, Wen-Hao Liu, Zhuo Li
- *Cadence Design Systems, Inc.*

Charles J. Alpert - *Cadence Design Systems, Inc.*

David Z. Pan - *Univ. of Texas at Austin*

1C.2 **OWARU: Free Space-Aware Timing-Driven Incremental Placement**

Jinwook Jung - *Korea Advanced Institute of Science and Technology*

Gi-Joon Nam, Lakshmi Reddy - *IBM Research*

Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

Youngsoo Shin - *Korea Advanced Institute of Science and Technology*

1C.3 **Detailed Placement for Modern FPGAs using 2D Dynamic Programming**

Shounak Dhar - *Univ. of Texas at Austin*

Saurabh Adya, Love Singhal, Mahesh Iyer - *Intel Corp.*

David Z. Pan - *Univ. of Texas at Austin*

Special Session 1D - Emerging Technologies and Hardware Security: Prospects and Challenges

Time: 10:30am - 12:00pm | Room: Phoenix North

Moderator:

Serge Leef - *Mentor Graphics Corp.*

Organizers:

Swaroop Ghosh - *Pennsylvania State Univ.*

Ramesh Karri - *New York Univ.*

Emerging technologies have surfaced to assist the CMOS technology in several ways such as performance, energy-efficiency to continue on scaling path. Interestingly, these technologies have also demonstrated several properties that could be undesirable for circuit design but could be extremely useful for security. It is important to examine these less-understood properties from a security perspective to determine their right applications ranging from attack prevention and forensics. This special session will present the security dimensions of emerging non-volatile memories, nano-materials and nanotechnologies. It will attempt to uncover both sides of the coin - the prospects of emerging technologies to aide in hardware security as well as new challenges that may surface due adoption of emerging technologies.

- 1D.1 Security and Privacy Threats to On-Chip Non-Volatile Memories and Countermeasures**
Swaroop Ghosh, Md. Nasim Imtiaz Khan, Asmit De, Jae-won Jang - *Pennsylvania State Univ.*
- 1D.2 Security Engineering of Nanostructures and Nanomaterials**
Davood Shahrjerdi, Bayan Nasri, Darren Armstrong, Abdullah S. Alharbi, Ramesh Karri
 - *New York Univ.*
- 1D.3 Hardware security primitives enabled by emerging memories**
An Chen - *Semiconductor Research Corp. & IBM Research*

ACM Student Research Competition Poster Session

Time: 11:30am - 1:30pm | Room: Dover's

Sponsored by Microsoft Research, the ACM Student Research Competition (SRC) is an internationally recognized venue enabling undergraduate and graduate students who are members of ACM and ACM SIGDA to:

- Experience the research world—for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees.
- Rub shoulders with academic and industry luminaries.
- Understand the practical applications of their research.
- Perfect their communication skills.
- Receive prizes and gain recognition from ACM, and the greater computing community.

ACM SRC has three rounds:

- (1) abstract review
- (2) poster session (this session)
- (3) technical presentation

In the first round, 2-page research abstracts are evaluated by EDA experts from academia and industry to select participants for the second round (this session). For the ACM SRC at ICCAD 2015 competition, 20 participants were selected to present their research at ICCAD.

The posters are evaluated by EDA experts to select up to 5 participants in graduate and undergraduate categories to advance to the final round (technical presentation round). Students are expected to discuss their work with judges. Each judge will rate the student's visual presentation based on the criteria of uniqueness of the approach, the significance of the contribution, visual presentation, and quality of presentation.

More details can be found at: sigda.org/src

Sponsored by:



Lunch

Time: 12:15pm - 1:15pm | Room: Phoenix Central

Join fellow attendees for lunch in Phoenix Central.

2A - Accelerators and Design Methodologies for Brain-inspired Computing

Time: 1:30pm - 3:30pm | Room: Phoenix South

Moderator:

Gayatri Mehta - *Univ. of North Texas*

The focus of this session is on accelerators and design methodologies for neuro-inspired computing. The session starts with "Caffeine", which describes a technique for accelerating deep neural networks using FPGAs. It integrates the design flow with Caffe to provide a comprehensive design framework for FPGA implementations. The "Memsqueezer" paper focuses on compressing weights and intermediate data of deep neural networks to reduce storage and to accelerate computation. The third paper proposes a hardware/software co-design framework for a sparse matrix vector multiplication accelerator. In particular, it discusses a novel way to partition matrix computation into multiple processing elements to improve data locality. The last paper presents a compact oscillation neuron based on metal-insulator-transition and its use in neuromorphic computing systems.

2A.1 **Caffeine: Towards Uniformed Representation and Acceleration for Deep Convolutional Neural Networks**

Chen Zhang - *Peking Univ.*

Zhenman Fang, **Peipei Zhou** - *Univ. of California, Los Angeles*

Peichen Pan - *Falcon Computing Solutions, Inc.*

Jason Cong - *Univ. of California, Los Angeles*

2A.2 **Re-architecting the On-chip memory Sub-system of Machine-Learning Accelerator for Embedded Devices**

Ying Wang, Huawei Li, Xiaowei Li - *Chinese Academy of Sciences*

2A.3 **A Data Locality-aware Design Framework for Reconfigurable Sparse Matrix-Vector Multiplication Kernel**

Sicheng Li, Yandan Wang - *Univ. of Pittsburgh*

Wujie Wen - *Florida International Univ.*

Yu Wang - *Tsinghua Univ.*

Yiran Chen, Hai (Helen) Li - *Univ. of Pittsburgh*

2A.4 **Compact Oscillation Neuron Exploiting Metal-Insulator-Transition for Neuromorphic Computing**

Pai-Yu Chen, Jae-sun Seo, Yu Cao, **Shimeng Yu** - *Arizona State Univ.*

2B - Advanced Simulation Techniques and Optimization of Analog/RF Circuits

Time: 1:30pm - 3:30pm | Room: Austin

Moderator:

Laleh Behjat - *Univ. of Calgary*

With the growing prevalence of interconnectedness of devices and sensors, the design and simulation of analog and RF circuits continues to be critical. The first paper in this session describes a combination of techniques for simulating electrical and thermal aspects together. The second paper presents a new decomposition technique which allows Volterra expansions to be extendable to strongly non-linear circuits. The third paper presents a scalable technique including correlations for predicting failure of rare events. The final paper in the session describes an optimization technique that explores both performance and parameter space simultaneously using randomized trees to find the solution.

2B.1 **A New Tightly-Coupled Transient Electro-Thermal Simulation Method for Power Electronics**

Quan Chen - *Univ. of Hong Kong*

Wim Schoenmaker - *Magwel*

2B.2 **A Tensor-Based Volterra Series Black-Box Nonlinear System Identification And Simulation Framework**

Kim Batselier, Zhongming Chen - *Univ. of Hong Kong*

Haotian Liu - *Cadence Design Systems, Inc.*

Ngai Wong - *Univ. of Hong Kong*

2B.3 **Efficient Statistical Analysis for Correlated Rare Failure Events via Asymptotic Probability Approximation**

Handi Yu, **Jun Tao**, Changhai Liao, Yangfeng Su - *Fudan Univ.*

Dian Zhou - *Univ. of Texas at Dallas*

Xuan Zeng - *Fudan Univ.*

Xin Li - *Carnegie Mellon Univ.*

2B.4 **Duplex: Simultaneous Parameter-Performance Exploration for Optimizing Analog Circuits**

Seyed Nematollah Ahmadyan, Shobha Vasudevan - *Univ. of Illinois at Urbana-Champaign*

2C - Routing and Clocking

Time: 1:30pm - 3:30pm | Room: Robertson

Moderator:

Mehmet Yildiz - *Cadence Design Systems, Inc.*

In this session, new algorithms for global routing, PCB routing, redistribution layer (RDL) routing, as well as flip-flop tray synthesis are presented. The session starts with a new flip flop clustering arrangement as big multi-bit trays for power reduction.

Next, a global routing algorithm, which packs RC-aware global wires with respect to global timing constraints, is presented. In the third paper, a SAT modulo theory solver is used to perform scalable PCB escape routing. Finally, for the last paper, a new approach for multi-chip and multi-layer RDL routing is given.

***2C.1 Improved Flop Tray-Based Design Implementation for Power Reduction**

Andrew B. Kahng, **Jiajia Li**, Lutong Wang - *Univ. of California at San Diego*

2C.2 RC-Aware Global Routing

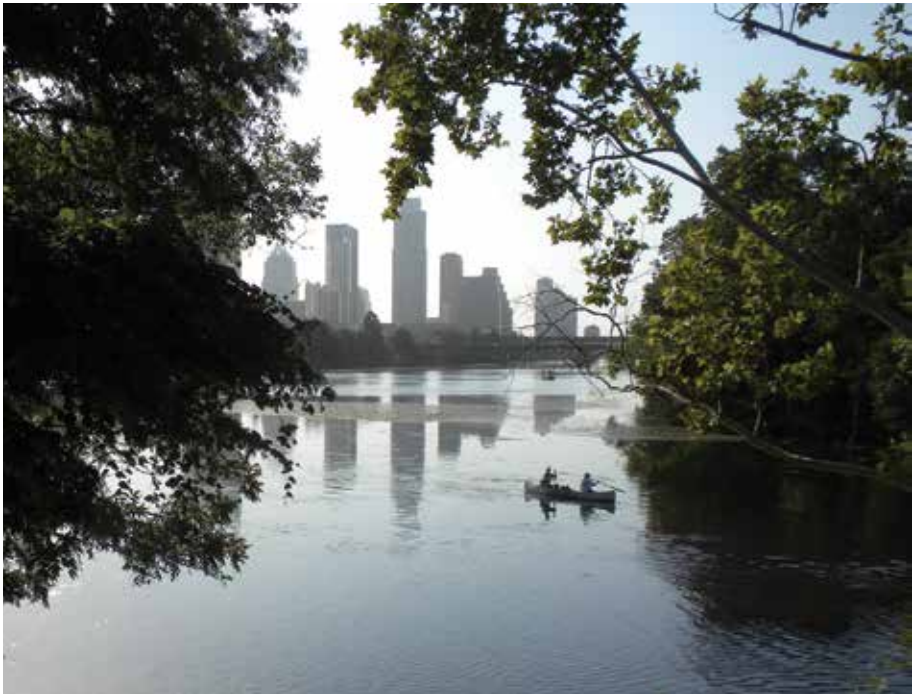
Rudolf Scheifele - *Univ. of Bonn*

2C.3 Scalable, High-Quality SAT-Based Multi-Layer Escape Routing

Sam Bayless, Holger H. Hoos, Alan J. Hu - *Univ. of British Columbia*

2C.4 Redistribution Layer Routing for Integrated Fan-Out Wafer-Level Chip-Scale Packages

Bo-Qiao Lin, Ting-Chou Lin, Yao-Wen Chang - *National Taiwan Univ.*



All speakers are denoted in bold | * denotes Best Paper Candidate

Special Session 2D - Future Value in ICs: Who Will Deliver It, and How

Time: 1:30pm - 3:30pm | Room: Phoenix North

Moderator:

Shishpal Rawat - *Council on EDA*

While system value today is increasingly achieved in a “beyond-Moore” sense, it is unknown how to measure and credit “progress” of DA, architectures, circuits/devices, patterning, etc. with respect to product-level benefits. Thus, it is very challenging for industry, academia and funding entities to envision, and to define, R&D objectives and prioritizations. In particular, the credit and value accorded to EDA technology has always been a sore point for professionals and researchers in the field. This special session will be about IC product value in a holistic sense, along with ‘credit assignment’ across the electronics/semiconductor industry stack. The goal is to spark improved understanding of what will be valuable for researchers and practitioners to work on. Four invited talks will give perspectives on how progress should be defined, and how it should be assessed – across levels of architecture, circuit, physical implementation, and underlying device/process technology.

2D.1 The Architecture Value Engine: Measuring and Delivering Sustainable SoC Improvement

Juan-Antonio Carballo - *Advanced Micro Devices, Inc.*

Bangqi Xu - *Univ. of California at San Diego*

2D.2 Circuit Valorization in the IC Design Ecosystem

Jose Pineda de Gyvez, Hamed Fatemi - *NXP Semiconductors*

Maarten Vertregt - *NXP Semiconductors*

2D.3 Interconnect-aware Device Targeting from PPA Perspective

Mustafa Badaroglu - *Qualcomm Europe, Inc.*

Jeff Xu - *Qualcomm Technologies, Inc.*

2D.4 Measuring Progress and Value of IC Implementation Technology

Andrew B. Kahng, Hyein Lee, Jiajia Li - *Univ. of California at San Diego*

3A - Camouflaging and Obfuscation

Time: 4:00pm - 5:30pm | Room: Phoenix South

Moderator:

Srinivas Patil - *Qualcomm Technologies, Inc.*

It is now relatively easy to fully reverse engineer the hardware design from a physical chip. Circuit camouflaging and logic obfuscation attempt to thwart such reverse engineering attacks. This session has three papers describing the state-of-the-art techniques to protect your hardware design.

3A.1 Provably Secure Camouflaging Strategy for IC Protection

Meng Li - *Univ. of Texas at Austin*

Kaveh Shamsi, Travis Meade - *Univ. of Central Florida*

Zheng Zhao - *Univ. of Texas at Austin*

Bei Yu - *Chinese Univ. of Hong Kong*

Yier Jin - *Univ. of Central Florida*

David Z. Pan - *Univ. of Texas at Austin*

3A.2 CamoPerturb: Secure IC Camouflaging for Minterm Protection

Muhammad Yasin - *New York Univ.*

Bodhisatwa Mazumdar, Ozgur Sinanoglu - *New York Univ., Abu Dhabi*

Jeyavijayan Rajendran - *Univ. of Texas at Dallas*

3A.3 Chip Editor: Leveraging Circuit Edit for Logic Obfuscation and Trusted Fabrication

Bicky Shakya, Navid Asadizanjani, Domenic Forte, Mark Tehranipoor - *Univ. of Florida*

3B - Optimizing Memory and Flip-flops

Time: 4:00pm - 5:30pm | Room: Austin

Moderator:

Muhammad Shafique - *Technische Univ. Wien*

In this session, we present three exciting developments in the use of memory in HLS, and optimization of multi-bit flip-flops. The first paper discusses an efficient way to organize memory access in streaming applications. The next paper targets efficient data access in multi-bank memories. The final paper presents an efficient synthesis scheme for multi-bit flip-flops.

3B.1 Arbitrary Streaming Permutations with Minimum Memory and Latency

Thaddeus Koehn, Peter Athanas - *Virginia Polytechnic Institute and State Univ.*

3B.2 Multi-bank Memory Optimization for Parallel Data Access in Multiple Data Arrays

Shouyi Yin, **Zhicong Xie**, Chenyue Meng, Leibo Liu, Shaojun Wei - *Tsinghua Univ.*

3B.3 Allocation of Multi-bit Flip-flops in Logic Synthesis for Power Optimization

Dongyoun Yi, Taewhan Kim - *Seoul National Univ.*

Special Session 3C - Design Automation for Next-Generation Automotive Systems

Time: 4:00pm - 6:00pm | Room: Robertson

Moderator:

Qi Zhu - *Univ. of California, Riverside*

Organizer:

Qi Zhu - *Univ. of California, Riverside*

The four invited talks in this session address some of the key challenges for next-generation automotive systems, and demonstrate the importance and value of design automation techniques for future automotive design. These include a novel methodology for automotive controller design with consideration of computation, communication and memory issues; virtualization-based testing techniques for fast development of automotive control, software and hardware; a statistical methodology for validating machine learning systems for autonomous driving; and a cross-layer framework for modeling, exploration and validation of connected vehicles.

3C.1 Model-based Design of Resource-efficient Automotive Control Software

Wanli Chang - *Singapore Institute of Technology*

Debayan Roy, Licong Zhang, **Samarjit Chakraborty** - *Technische Univ. München*

3C.2 Testing Automotive Embedded Systems under X-in-the-Loop Setups

Ghizlane Tibba, Christoph Malz, Christoph Stoermer, Natarajan Nagarajan - *ETAS GmbH*

Licong Zhang, Samarjit Chakraborty - *Technische Univ. München*

3C.3 Efficient Statistical Validation of Machine Learning Systems for Autonomous Driving

Weijing Shi, Mohamed Baker Alawieh, **Xin Li** - *Carnegie Mellon Univ.*

Huafeng Yu - *Boeing*

Nikos Arechiga, Nobuyuki Tomatsu - *Toyota InfoTechnology Center*

3C.4 CONVINCE: A Cross-Layer Modeling, Exploration and Validation Framework for Next-Generation Connected Vehicles

Bowen Zheng - *Univ. of California, Riverside*

Chung-Wei Lin - *Toyota InfoTechnology Center*

Huafeng Yu - *Boeing*

Hengyi Liang, Qi Zhu - *Univ. of California, Riverside*

Special Session 3D - 2016 CAD Contest

Time: 4:00pm - 6:00pm | Room: Phoenix North

Moderators:

Shih-Hsu Huang - *Chung Yuan Christian Univ.*
Rung-Bin Lin - *Yuan Ze Univ.*

Organizers:

Shih-Hsu Huang - *Chung Yuan Christian Univ.*
Rung-Bin Lin - *Yuan Ze Univ.*
Myung-Chul Kim - *IBM Corp.*
Shigetoshi Nakatake - *Univ. of Kitakyushu*

The CAD Contests at ICCAD and associated benchmark suites have been instrumental in advancing the state-of-the-art in EDA. Additionally, they have fostered productive industry-academia collaboration. In its fifth year, the 2016 CAD Contest is among the largest worldwide EDA contests, attracting 135 teams from 11 regions/countries. Three contest problems in the areas of design verification, logic synthesis, and design for manufacturing are called for competition this year. This session gives an overview of the 2016 CAD Contest, presents the three contest problems, releases the associated benchmarks, and announces the winners. It also provides a venue for the top-performing teams to showcase their key ideas via short video presentations. Based on the momentum accumulated by EDA contests, the last talk concludes this session by proposing an OpenDesign Flow Database, which provides an infrastructure for VLSI design and design automation research.

3D.1 Overview of the 2016 CAD Contest at ICCAD

Shih-Hsu Huang - *Chung Yuan Christian Univ.*
Rung-Bin Lin - *Yuan Ze Univ.*
Myung-Chul Kim - *IBM Corp.*
Shigetoshi Nakatake - *Univ. of Kitakyushu*

3D.2 ICCAD-2016 CAD Contest in Large-scale Identical Fault Search

Tien-Chun (Tangent) Wei, Kuo-Ching (Luke) Lin - *Synopsys Taiwan Co., Ltd.*

3D.3 ICCAD-2016 CAD Contest in Non-exact Projective NPNP Boolean Matching and Benchmark Suite

Chi-An (Rocky) Wu, Chih-Jen (Jacky) Hsu - *Cadence Taiwan, Inc.*
Kei-Yong Khoo - *Cadence Design Systems, Inc.*

3D.4 ICCAD-2016 CAD Contest in Pattern Classification for Integrated Circuit Design Space Analysis and Benchmark Suite

Rasit O. Topaloglu - *IBM Corp.*

3D.5 OpenDesign Flow Database: The Infrastructure for VLSI Design and Design Automation Research

Jinwook Jung - *Korea Advanced Institute of Science and Technology*
Iris Hui-Ru Jiang - *National Chiao Tung Univ.*
Gi-Joon Nam, Victor N. Kravets - *IBM T.J. Watson Research Center*
Laleh Behjat - *Univ. of Calgary*
Yih-Lang Li - *National Chiao Tung Univ.*

Sponsored by:



Networking Reception

Time: 5:30pm - 6:15pm | Room: Phoenix Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

ACM Student Research Competition Technical Presentations

Time: 6:00pm - 8:00pm | Room: Phoenix South

The ACM Student Research Competition allows both graduate and undergraduate students to discuss their research with student peers, as well as academic and industry researchers, in an informal setting, while enabling them to attend ICCAD.

This session is the final round of ACM SRC at ICCAD 2016. Each student will present for 10 minutes, followed by a 5-minute question and answer period. This session will be attended by the evaluators and any interested conference attendees. The top three winners in each category will be chosen based on these presentations.

The undergraduate and graduate finalists will be eligible to compete in the ACM SRC Grand Finals to be held in June 2017. More details can be found at: sigda.org/src

Sponsored by:



Cadence Sponsored Presentation

Time: 6:15pm - 8:00pm | Room: Phoenix Central

Sponsored by:



- TUESDAY SCHEDULE -

8:30 - 10:30am

Session 4A: Catch the Trojans and Shield the PUFs

Room: Phoenix South

Session 4B: Litho-aware Design for Manufacturability: Present and Future

Room: Austin

Session 4C: Symbolic Bug Hunting, Diagnosis and Fault Propagation

Room: Robertson

Embedded Tutorial 4D: Going Vertical: Roadmap for Energy-Efficient and Reliable Massive-Scale Computing based on 3D Integration

Room: Phoenix North

10:30 - 11:00am

Coffee Break

Room: Prefunction Foyer

11:00am - 12:30pm

Session 5A: Building Efficient Software for Next Generation Embedded Systems

Room: Phoenix South

Session 5B: Tolerating Low Power Designs

Room: Austin

Special Session 5C: Routability-Driven FPGA Placement

Room: Robertson

Special Session 5D: Reliability Mitigation and Resiliency-Aware Design for Energy-Efficient Systems

Room: Phoenix North

12:45 - 1:45pm

Tuesday Invited Luncheon Keynote: Socially Acceptable AI-based City Driving

Room: Phoenix Central

Sponsored by:



IEEE



IEEE Council on Electronic Design Automation

2:00 - 4:00pm

Session 6A: Flying, Folding, Learning, and Spying: the Emerging CPS Design Challenges

Room: Phoenix South

Session 6B: System Design Methods for Computational Efficiency

Room: Austin

Session 6C: Approximate Hardware Design

Room: Robertson

Special Session 6D: New Application Frontiers for Formal Verification

Room: Phoenix North

4:00 - 4:30pm

Coffee Break

Room: Prefunction Foyer

4:30 - 6:00pm

Session 7A: Optimization Techniques for 3D-ICs, DFM and Yield Estimation

Room: Phoenix South

Session 7B: Fab Attestation and Split Manufacturing

Room: Austin

Embedded Tutorial 7C: OpenRAM: An Open-Source Memory Compiler

Room: Robertson

Panel 7D: Challenges and Opportunities of Stochastic Computing in the Dusk of Moore's Law and the Dawn of Big Data

Room: Phoenix North

6:00 - 6:30pm

Networking Reception

Room: Phoenix Foyer

6:30 - 8:00pm

ACM/SIGDA Member Meeting

Room: Phoenix Central

Sponsored by:



4A - Catch the Trojans and Shield the PUFs

Time: 8:30am - 10:30am | Room: Phoenix South

Moderator:

Yier Jin - *Univ. of Central Florida*

Trojan insertion, cloning, tampering and reverse engineering are some of the top issues in hardware security. This session will cover: (i) innovative techniques to catch stealthy Trojans; and, (ii) attack-resilient authentication primitives such as Physically Unclonable Functions (PUFs).

***4A.1 Malicious LUT: A Stealthy FPGA Trojan Injected and Triggered by the Design Flow**
Christian Krieg, Clifford Wolf, Axel Jantsch - *Technische Univ. Wien*

4A.2 On Detecting Delay Anomalies Introduced by Hardware Trojans

Dylan Ismari - *Univ. of New Mexico*

Charles Lamech - *Intel Corp.*

Swarup Bhunia - *Univ. of Florida*

Fareena Saqib - *Florida Institute of Technology*

Jim Plusquellic - *Univ. of New Mexico*

4A.3 An Optimization-Theoretic Approach for Attacking Physical Unclonable Functions
Yuntao Liu, Yang Xie, Chongxi Bao, Ankur Srivastava - *Univ. of Maryland*

4A.4 LRR-DPUF: Learning Resilient and Reliable Digital Physical Unclonable Function

Jin Miao - *Cadence Design Systems, Inc.*

Meng Li - *Univ. of Texas at Austin*

Subhendu Roy - *Cadence Design Systems, Inc.*

Bei Yu - *Chinese Univ. of Hong Kong*

4B - Litho-aware Design for Manufacturability: Present and Future

Time: 8:30am - 10:30am | Room: Austin

Moderator:

Iris Hui-Ru Jiang - *National Chiao Tung Univ.*

This session is devoted to litho-aware DfM techniques addressing issues of litho-aware routing, hotspot detection, and directed self assembly (DSA). The first paper proposes a novel online learning algorithm for hotspot detection. The second paper deals with the problem of cut redistribution in 1D gridded design using mask assignment. Finally, the last two papers in this session address DSA-aware routing.

4B.1 Enabling Online Learning in Lithography Hotspot Detection with Information-theoretic Feature Optimization

Hang Zhang, Bei Yu, Evangeline F.Y. Young - *Chinese Univ. of Hong Kong*

4B.2 Incorporating Cut Redistribution with Mask Assignment to Enable 1D Gridded Design

Jian Kuang, **Evangeline F.Y. Young**, Bei Yu - *Chinese Univ. of Hong Kong*

4B.3 VCR: Simultaneous Via-template and Cut-template-aware Routing for Directed Self-Assembly Technology

Yu-Hsuan Su, Yao-Wen Chang - *National Taiwan Univ.*

4B.4 DSA-compliant Routing for Two-dimensional Patterns Using Block Copolymer Lithography

Yu-Hsuan Su, Yao-Wen Chang - *National Taiwan Univ.*

4C - Symbolic Bug Hunting, Diagnosis and Fault Propagation

Time: 8:30am - 10:30am | Room: Robertson

Moderator:

Ian G. Harris - *Univ. of California, Irvine*

This session presents a range of symbolic techniques for the detection and analysis of bugs. The first two papers discuss tools and techniques for finding design errors. The third paper introduces an exact approach for finding fault candidates in digital circuits. In the final paper a formal method to analyze the propagation of single event transients at the gate-level is presented.

4C.1 The Art of Semi-Formal Bug Hunting

Pradeep Kumar Nalla, RajKumar Gajavelly, Jason Baumgartner, Hari Mony, Robert Kanzelman, Alexander Ivrii - *IBM Corp.*

4C.2 Compiled Symbolic Simulation for SystemC

Vladimir Herdt, Hoang M. Le - *Univ. of Bremen*
Daniel Grosse, Rolf Drechsler - *Univ. of Bremen & DFKI GmbH*

4C.3 Exact Diagnosis using Boolean Satisfiability

Heinz Riener - *German Aerospace Center*
Goerschwin Fey - *Univ. of Bremen*

4C.4 Efficient and Accurate Analysis of Single Event Transients Propagation Using SMT-Based Techniques

Ghaith Bany Hamad - *École Polytechnique de Montréal*
Ghaith Kazma, Otmane aït Mohamed - *Concordia Univ.*
Yvon Savaria - *École Polytechnique de Montréal*



All speakers are denoted in bold | * denotes Best Paper Candidate

Embedded Tutorial 4D - Going Vertical: Roadmap for Energy-Efficient and Reliable Massive-Scale Computing based on 3D Integration

Time: 8:30am - 10:30am | Room: Phoenix North

Moderator:

Umit Ogras - *Arizona State Univ.*

Organizer:

Krishnendu Chakrabarty - *Duke Univ.*

Three-dimensional (3D) integration based on through-silicon vias (TSVs), a breakthrough technology to achieve "More Moore and More Than Moore," provides higher performance, lower power consumption, and higher bandwidth by utilizing vertical interconnects and die/wafer stacking. In addition, emerging memory technologies such as 3D stacked memory and non-volatile memories (NVMs) provide a game-changing opportunity to rethink traditional system architectures for post-Moore computing systems. Advances in 3D integration enable us to design radically new on-chip interconnection fabrics that can support exascale computing by integrating a very large number of embedded cores. However, increasing packaging densities facilitated by 3D integration also exacerbate the problems of thermal management and power delivery. Moreover, there is an even greater need for reliable and fault-tolerant design methodologies to address TSV defects and TSV degradation due to aging and workload-induced stress. The tutorial describes recent advances in 3D integration, innovative 3D chip architectures, and design-for-testability techniques to overcome the major obstacles that impede the path towards exascale computing.

4D.1 Power Delivery in 3D Packages: Current Crowding Effects, Dynamic IR Drop and Compensation Network using Sensors

Sukeshwar Kannan - *GLOBALFOUNDRIES*

Mehdi Sadi - *Univ. of Florida*

Luke England - *GLOBALFOUNDRIES*

4D.2 Cost Analysis and Cost-Driven IP Reuse Methodology for SoC design Based on 2.5D/3D Integration

Dylan Stow, Itir Akgun, Peng Gu, Russell Barnes, **Yuan Xie**

- *Univ. of California, Santa Barbara*

4D.3 Energy-Efficient and Reliable 3D Network-on-Chip (NoC): Architectures and Optimization Algorithms

Sourav Das, Janardhan Rao Doppa, **Partha Pratim Pande** - *Washington State Univ.*

Krishnendu Chakrabarty - *Duke Univ.*

4D.4 The Hype, Myths, and Realities of Testing 3D Integrated Circuits

Ran Wang - *NVIDIA Corporation*

Sergej Deutsch, Mukesh Agrawal - *Intel Corp.*

Krishnendu Chakrabarty - *Duke Univ.*

5A - Building Efficient Software for Next Generation Embedded Systems

Time: 11:00am - 12:30pm | Room: Phoenix South

Moderator:

Jiang Hu - *Texas A&M Univ.*

This session focuses on recent trends in design and implementation of embedded systems and software. Embedded systems are resource constrained with performance characteristics like memory usage, timing, and power and performance continuing to dominate their design and implementation. Modern hardware architectural features like multi-core, pipelining and cache and the increased need for GPU requirements complicate the problem of efficient design and implementation. The three papers that appear in this session focus on these issues, proposing new and efficient solutions to some of these problems.

5A.1 TASA: Toolchain-Agnostic Static Software Randomisation for Critical Real-Time Systems

Leonidas Kosmidis, Roberto Vargas - *Univ. Politècnica de Catalunya & Barcelona Supercomputing Center*

David Morales, Eduardo Quiñones, Jaume Abella - *Barcelona Supercomputing Center*
Francisco J. Cazorla - *Barcelona Supercomputing Center & Spanish National Research Council*

5A.2 Splitting Functions in Code Management on Scratchpad Memories

Youngbin Kim - *Yonsei Univ.*

Jian Cai, Yooseong Kim - *Arizona State Univ.*

Kyoungwoo Lee - *Yonsei Univ.*

Aviral Shrivastava - *Arizona State Univ.*

5A.3 Adaptive Performance Prediction for Integrated GPUs

Ujjwal Gupta, Joseph Campbell, Umit Y. Ogras - *Arizona State Univ.*

Raid Ayoub, Michael Kishinevsky, Francesco Paterna - *Intel Corp.*

Suat Gumussoy - *IEEE*

5B - Tolerating Low Power Designs

Time: 11:00am - 12:30pm | Room: Austin

Moderator:

Ulf Schlichtmann - *Technische Univ. München*

Low power objectives often compromise reliability, and we need ways to strike a balance. The first paper in this session describes a fault tolerance approach for energy-efficient IoTs. The second paper tries to extend TTF by isolating critical paths in low supply voltage environments. The third paper presents control synthesis and delay sensing to achieve resilience in adaptive supply voltage designs.

5B.1 Energy-efficient Fault Tolerance Approach for Internet of Things Applications

Teng Xu, Miodrag Potkonjak - *Univ. of California, Los Angeles*

5B.2 Critical Path Isolation for Time-to-Failure Extension and Lower Voltage Operation

Yutaka Masuda, Masanori Hashimoto, Takao Onoye - *Osaka Univ.*

5B.3 Control Synthesis and Delay Sensor Deployment for Efficient ASV Designs

Chaofan Li - *Texas A&M Univ.*

Sachin Sapatnekar - *Univ. of Minnesota*

Jiang Hu - *Texas A&M Univ.*

Special Session 5C - Routability-Driven FPGA Placement

Time: 11:00am - 12:30pm | Room: Robertson

Moderator:

Stephen Yang - *Xilinx Inc.*

Organizer:

Evangeline F. Y. Young - *Chinese Univ. of Hong Kong*

Field Programmable Gate Arrays (FPGA) finds wider applications nowadays with the advancement in technology. New generations of FPGA target at implementing the whole system on a single device, and various resources like LUT, flip-flop, RAM, DSP are placed at different locations of the device. The trend is bigger and faster in general. These advances in FPGA technology have posed many new challenges to the design tools. FPGA tools nowadays need to handle various objectives like power, timing, routability and wire length, on top of other challenges like clock net construction, resource allocation, run time reduction, etc. This session highlights new placement frameworks and techniques for today's large scale heterogeneous FPGAs. There will be four talks in the session, including one from company giving industrial perspectives on new routing issues on today's large scale multi-layers heterogeneous FPGA devices and architectures. With the advances of FPGA technology, there arise many new challenges and problems that will interest academia and stimulate more research and explorations. The other three talks will be coming from the top three winning teams of the Routability-driven FPGA Placement Contest held in ACM International Symposium on Physical Design 2016. Their talks will feature various techniques in dealing with FPGA specific placement problems like congestion aware packing, routability-driven placement, FPGA-based routing estimation and detailed placement, etc. Various techniques from traditional FPGA placement research and standard cell/mixed-size placement research will meet here, moving forward research to make possible effective and efficient FPGA placement methodologies.

5C.1 Performance Driven Routing for Modern FPGAs

Parivallal Kannan, Satish Sivaswamy - *Xilinx Inc.*

5C.2 UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing

Wuxi Li, Shounak Dhar, David Z. Pan - *Univ. of Texas at Austin*

5C.3 RippleFPGA: A Routability-Driven Placement for Large-Scale Heterogeneous FPGAs

Chak-Wa Pui, Gengjie Chen, Wing-Kai Chow, Ka-Chun Lam, Jian Kuang, Peishan Tu, Hang Zhang, Evangeline F.Y. Young, Bei Yu - *Chinese Univ. of Hong Kong*

5C.4 GPlace - A Congestion-aware Placement tool for UltraScale FPGAs

Ryan Pattison, **Ziad Abuowaimer**, Shawki Areibi, Gary Grewal, Anthony Vannelli - *Univ. of Guelph*

Special Session 5D - Reliability Mitigation and Resiliency-Aware Design for Energy-Efficient Systems

Time: 11:00am - 12:30pm | Room: Phoenix North

Moderators:

Ertugrul Demircan - *NXP Semiconductors*

Organizer:

Sheldon Tan - *Univ. of California, Riverside*

Reliability has become a significant challenge for design of current nanometer integrated circuits (ICs). It is expected that future chips will show signs of reliability-induced age much faster than the previous generations. Furthermore, long-term reliability degradation caused by aging effects are becoming a limiting constraint in emerging computing platforms such as dark silicons, mobile devices and emerging FinFET devices due to increased failure rates. Semiconductor industry faces new challenges to maintain the reliability in the reality of ever-continued increase in the die size and number of transistors accompanying by the performance driven down-scaling in transistor size. Additionally, in ultra-low-power systems, aggressive energy efficiency can aggravate some of these reliability challenges. To mitigate the increasing reliability and resiliency problems, holistic solutions starting from physics, circuit to all the way to system levels are desired. This special session tries to address the increasing reliability and resiliency issues of low-power VLSI ICs. It consists of three presentations covering both transient soft-error and long-term hard reliability issues, resiliency improvement techniques for low power systems ranging from modeling, assessment, optimization and dynamic management at system levels.

5D.1 Resiliency in Dynamically Power Managed Designs

Liangzhen Lai, Vikas Chandra, Rob Aitken - *ARM, Inc.*

5D.2 Dynamic Reliability Management for Near-Threshold Dark Silicon Processors

Taeyoung Kim, Zeyu Sun, Chase Cook, Jagadeesh Gaddipati - *Univ. of California, Riverside*

Hai Wang - *Univ. of Electronic Science and Technology of China*

Haibao Chen - *Shanghai Jiao Tong Univ.*

Sheldon Tan - *Univ. of California, Riverside*

5D.3 A Cross-Layer Approach for Resiliency and Energy Efficiency in Near Threshold Computing

Mohammad Saber Golanbari, Anteneh Gebregiorgis, Fabian Oboril, Saman Kiamehr,

Mehdi Tahoori - *Karlsruhe Institute of Technology*



Tuesday Invited Luncheon Keynote: Socially Acceptable AI-based City Driving

Time: 12:45pm - 1:45pm | Room: Phoenix Central

Speaker:

Maarten Sierhuis - *Nissan Research Center, Silicon Valley*

Autonomous vehicles are standing at our doorstep as a big innovation, not only for automobile industry, but also for our society as a whole. Like any technology, it is very important that we develop it using a human-centered approach. For autonomous vehicles this means that we need to develop the technology in such a way that it is "socially acceptable." In other words, people understand and accept how our autonomous vehicles behave on the road, together with other road users. This is the case for driving autonomously on our highways, but will be even more the case when autonomous vehicles will drive in urban environments and in our city centers. In this talk I will describe Nissan's roadmap for bringing autonomous vehicles to market, as well as how we are researching the human-centered development of autonomous vehicles.

Biography:

Dr. Maarten Sierhuis leads a team of researchers at Nissan's Research Center in Silicon Valley, tasked with developing autonomous vehicles (AVs), connected vehicles (CVs) and Human-Machine Interaction and Interfaces (HMI2). As a former NASA research scientist, he spent the bulk of his career creating autonomous technology for space exploration. Now he brings his expertise down to earth to help shape the future of motoring and how people will interact with intelligent cars capable of driving themselves.

Maarten is responsible for developing the Artificial Intelligence (AI) software for Nissan's AVs. The role also entails researching the technology required to create connected vehicles, and to allow people to interact with AVs. Finding the talent to bring these dreams to reality is a key aspect of his job.

Born in the Netherlands, Maarten has lived all over the world, including periods in the US, Nigeria, Suriname, Saudi Arabia and Italy. He was educated in the Netherlands, reading computer science as an undergraduate at the Polytechnic University in The Hague, before achieving a PhD in Artificial Intelligence at the University of Amsterdam. He has worked at IBM, NYNEX and PARC. However, his most notable achievements were during a 12-year career at NASA, where he created a computer language that was used to develop an intelligent system for all communication between Mission Control and the International Space Station. He also developed an autonomous system to monitor and give advice to astronauts during spacewalks. "I look at a car the same way and astronaut looks at his spacesuit," he said. "It's your life support, your home and it's your work environment. This vision is what I bring to Nissan from NASA." He joined Nissan in February 2013 as Director of the Nissan Research Center in Silicon Valley, having lived in the San Francisco area for more than 16 years.

Sponsored by:  **IEEE**  **CEDA**
IEEE Council on Electronic Design Automation

6A - Flying, Folding, Learning, and Spying: the Emerging CPS Design Challenges

Time: 2:00pm - 4:00pm | Room: Phoenix South

Moderator:

Shiyan Hu - *Michigan Technological Univ.*

Current methodologies are not capable of designing for aerial and foldable devices. Even worse, security and learning ignore the physical aspects of Cyber-Physical Systems. This session presents four novel approaches for designing CPS. The first paper discusses the management of a fleet of drones, the second the trade off between power and flexibility in printed electronics, the third estimates the side channel emissions of 3D printers, and the fourth advances machine learning for wearable applications.

- 6A.1 Design Space Exploration of Drone Infrastructure for Large-Scale Delivery Services**
Sangyoung Park, Licong Zhang, Samarjit Chakraborty - *Technische Univ. München*
- 6A.2 Multi-Objective Design Optimization for Flexible Hybrid Electronics**
Ganapati Bhat, Ujjwal Gupta, Nicholas Tran, Jaehyun Park, Sule Ozev, Umit Y. Ogras
 - *Arizona State Univ.*
- 6A.3 KCAD: Kinetic Cyber Attack Detection Method for Cyber-Physical Additive Manufacturing Systems**
Sujit Rokka Chhetri - *Univ. of California, Irvine*
 Arquimedes Canedo - *Siemens Corp.*
 Mohammad Al Faruque - *Univ. of California, Irvine*
- 6A.4 Autonomous Sensor-Context Learning in Dynamic Human-Centered Internet-of-Things Environments**
Seyed Ali Rokni, Hassan Ghasemzadeh - *Washington State Univ.*

6B - System Design Methods for Computational Efficiency

Time: 2:00pm - 4:00pm | Room: Austin

Moderator:

Hiroyuki Tomiyama - *Ritsumeikan Univ.*

The session covers different methods for computational efficiency in various aspects of system design. The first paper presents a technique to improve the efficiency of design space exploration via SAT-based formulations of architectural constraints. The second paper proposes a hardware acceleration methodology for Iterative Stencil Loops. The third paper introduces a methodology to design low power neural networks with reduced requirements of memory and computational resources. The last paper proposes an automated framework for high speed code-specific CPU profiling that provides power and performance back-annotation.

6B.1 Formulating Customized Specifications for Resource Allocation Problem of Distributed Embedded Systems

Xinhai Zhang, Lei Feng, Martin Törngren, De-Jiu Chen - *KTH Royal Institute of Technology*

6B.2 A Polyhedral Model-based Framework for Dataflow Implementation on FPGA devices of Iterative Stencil Loops

Giuseppe Natale - *Politecnico di Milano*

Giulio Stramondo - *Politecnico di Milano & Univ. of Amsterdam*

Pietro Bressana, Riccardo Cattaneo, Donatella Sciuto, Marco D. Santambrogio
- *Politecnico di Milano*

6B.3 Efficient Memory Compression in Deep Neural Networks Using Coarse-Grain Sparsification for Speech Applications

Deepak Kadetotad, Sairam Arunachalam, Chaitali Chakrabarti, Jae-sun Seo

- *Arizona State Univ.*

6B.4 Parallel Code-Specific CPU Simulation with Dynamic Phase Convergence Modeling for HW/SW Co-Design

Warren Kemmerer, **Wei Zuo**, Deming Chen - *Univ. of Illinois at Urbana-Champaign*



All speakers are denoted in bold | * denotes Best Paper Candidate

6C - Approximate Hardware Design

Time: 2:00pm - 4:00pm | Room: Robertson

Moderator:

Michael Orshansky - *Univ. of Texas at Austin*

This session introduces new design methodologies for approximate computing. The first paper describes the architectural exploration of approximate multipliers. The second paper proposes the use of approximate multipliers in neural networks to improve energy efficiency. The third paper proposes an efficient technique and automated design tool for error prediction in approximate sequential circuits. The final paper introduces an automated synthesis approach for approximate circuits based on And-Inverter Graphs.

6C.1 Architectural-Space Exploration of Approximate Multipliers

Semeen Rehman - *Technische Univ. Dresden*

Walaa El-Harouni - *Karlsruhe Institute of Technology*

Muhammad Shafique - *Technische Univ. Wien*

Akash Kumar - *Technische Univ. Dresden*

Jörg Henkel - *Karlsruhe Institute of Technology*

6C.2 Design of Power-Efficient Approximate Multipliers for Approximate Artificial Neural Network

Vojtech Mrazek - *Brno Univ. of Technology*

Syed Shakib Sarwar - *Purdue Univ.*

Lukas Sekanina, Zdenek Vasicek - *Brno Univ. of Technology*

Kaushik Roy - *Purdue Univ.*

6C.3 Automated Error Prediction for Approximate Sequential Circuits

Amrut Kapare - *Univ. of Minnesota*

Hari Cherupalli - *Univ. of Minnesota, Twin Cities*

John Sartori - *Univ. of Minnesota*

6C.4 Approximation-aware Rewriting of AIGs for Error Tolerant Applications

Arun Chandrasekharan - *Univ. of Bremen*

Mathias Soeken - *École Polytechnique Fédérale de Lausanne*

Daniel Grosse, Rolf Drechsler - *Univ. of Bremen & DFKI GmbH*



All speakers are denoted in bold | * denotes Best Paper Candidate

Special Session 6D - New Application Frontiers for Formal Verification

Time: 2:00pm - 4:00pm | Room: Phoenix North

Moderator:

Daniel Große - *Univ. of Bremen & DFKI GmbH*

Organizers:

Wolfgang Ecker - *Infineon Technologies AG*

Ulf Schlichtmann - *Technical University of Munich*

The industrial usage of formal verification has grown substantially in recent years finally fulfilling an often stated claim of being a strong player in the verification area. However, the design and verification gap still widens due to new verification challenges such as verification of safety and security. Will formal techniques help further and make inroads in new, non-traditional applications areas? To address these questions, this session takes a look ahead and presents new application areas, where formal verification can be utilized in the future to improve verification productivity and to ensure even better design quality.

6D.1 QED and Symbolic QED: Dramatic Improvements in SoC Pre-silicon and Post-silicon Validation

Subhasish Mitra - *Stanford Univ.*

Clark Barrett - *New York Univ.*

6D.2 Properties First? A New Design Methodology for Hardware, and its Perspectives in Safety Analysis

Joakim Urdahl, Shrinidhi Udipi, Tobias Ludwig, Dominik Stoffel, **Wolfgang Kunz**

- *Univ. of Kaiserslautern*

6D.3 Where Formal Verification Can Help in Functional Safety Analysis

Alessandro Bernardini - *Technical University of Munich*

Wolfgang Ecker - *Infineon Technologies AG*

Ulf Schlichtmann - *Technical University of Munich*

6D.4 Formal Approaches to Design of Active Cell Balancing Architectures in Battery Management Systems

Sebastian Steinhorst - *Aarhus Univ.*

Martin Lukasiewicz - *TUM CREATE Ltd.*

7A - Optimization Techniques for 3D-ICs, DFM and Yield Estimation

Time: 4:30pm - 6:00pm | Room: Phoenix South

Moderator:

Duane Boning - *Massachusetts Institute of Technology*

This session highlights the use of optimization techniques for addressing emerging challenges in design for manufacturing, rare failure yield estimation, and 3D IC evaluation. The first paper considers the complex trade-offs between power, performance, cost, and yield in evaluating the benefits of monolithic 3D integrated circuits. The second paper proposes a unique dummy fill insertion framework based on sequential quadratic programming. Finally, the third paper proposes a systematic optimization approach for importance sampling that can be used for efficiently estimating the yield of SRAM bitcells with failure rates down to $1E-12$ and smaller.

7A.1 **How Much Cost Reduction Justifies the Adoption of Monolithic 3D ICs at 7nm Node?**

Bon Woong Ku - *Georgia Institute of Technology*

Peter Debacker - *IMEC*

Dragomir Milojevic - *Univ. Libre de Bruxelles*

Praveen Raghavan - *IMEC*

Sung Kyu Lim - *Georgia Institute of Technology*

7A.2 **A Novel Unified Dummy Fill Insertion Framework with SQP-Based Optimization Method**

Yudong Tao, Changhao Yan - *Fudan Univ.*

Yibo Lin - *Univ. of Texas at Austin*

Shengguo Wang - *Univ. of North Carolina, Charlotte*

David Z. Pan - *Univ. of Texas at Austin*

Xuan Zeng - *Fudan Univ.*

7A.3 **Efficient Yield Estimation through Generalized Importance Sampling with Application to NBL-Assisted SRAM bitcells**

Lorenzo Ciampolini - *STMicroelectronics*

Xavier Jonsson, Cyril Desclèves - *Mentor Graphics Corp.*

Jean-Christophe Lafont, Faress Tissafi Drissi, Jean-Paul Morin, David Turgis

- *STMicroelectronics*

Joseph Nguyen - *Grenoble Institute of Technology*

7B - Fab Attestation and Split Manufacturing

Time: 4:30pm - 6:00pm | Room: Austin

Moderator:

Swaroop Ghosh - *Pennsylvania State Univ.*

To compensate for the high costs of maintaining state-of-the-art fabrication facilities, the semiconductor industry has largely adopted a fab-less paradigm. This globalization has amplified concerns regarding the integrity of the electronics supply chain. Split manufacturing has been proposed as a promising way to mitigate these threats. The papers of this session investigate the security associated with split manufacturing, emerging devices conducive to split manufacturing, and novel methods for identifying the fabrication facility wherein an integrated circuit (IC) was manufactured.

7B.1 **Are Proximity Attacks a Threat to the Security of Split Manufacturing of Integrated Circuits?**

Jonathon C. Magaña - *Univ. of Wisconsin-Madison & Cardinal Stritch Univ.*

Daohang Shi, Azadeh Davoodi - *Univ. of Wisconsin-Madison*

7B.2 **Making Split-Fabrication More Secure**

Ping-Lin Yang, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara*

7B.3 **A Machine Learning Approach to Fab-of-Origin Attestation**

Ali Ahmadi, Mohammad-Mahdi Bidmeshki - *Univ. of Texas at Dallas*

Amit Nahar, Bob Orr, Michael Pas - *Texas Instruments, Inc.*

Yiorgos Makris - *Univ. of Texas at Dallas*

Embedded Tutorial 7C - OpenRAM: An Open-Source Memory Compiler

Time: 4:30pm - 6:00pm | Room: Robertson

Organizers:

Matthew Guthaus - *Univ. of California, Santa Cruz*

James Stine - *Oklahoma State Univ.*

Memory compilers have exploited memory regularity to automate design and layout of memory arrays for a long time. However, academic computer systems research is inhibited by the lack of a proper memory compiler. Expensive commercial solutions can provide memory models with immutable cells, limited configurations, and restrictive licenses. Manually creating memories can be time consuming and tedious and the designs are usually inflexible.

This tutorial introduces OpenRAM, an open-source memory compiler, that provides a framework for the generation, characterization, and verification of fabricable memory designs across various technologies, sizes, and configurations. OpenRAM provides reference circuit and physical implementations to aid research in computer architecture, system-on-chip design, memory circuit and device research, and computer-aided design.

OpenRAM itself is implemented in Python and is independent of commercial tools. It directly generates SPICE, GDSII, Verilog, LEF, and Liberty (.lib) timing models. It has a simple, flexible technology infrastructure that allows easy porting to new technologies and has been successfully ported to MOSIS SCMOS SCN3ME (0.5 μ m), NCSU FreePDK (45nm), IBM CMOS 8SF, and IBM CMOS 32nm SOI. This list contains both freely available academic processes and commercially fabricable technologies, as well. It is distributed only with setup for the freely available academic processes (SCMOS and FreePDK), but with little effort can be easily and readily expanded.

OpenRAM includes a memory characterizer that measures the timing and power characteristics through SPICE simulation. The characterizer generates the SPICE stimulus, written in standard SPICE format, and can be used with any simulator that supports this.

7C.1 OpenRAM: An Open-Source Memory Compiler

Matthew Guthaus - *Univ. of California, Santa Cruz*

James Stine, **Samira Ataei** - *Oklahoma State Univ.*

Brian Chen, Bin Wu - *Univ. of California, Santa Cruz*

Mehedi Sarwar - *Oklahoma State Univ.*

Panel 7D - Challenges and Opportunities of Stochastic Computing in the Dusk of Moore's Law and the Dawn of Big Data

Time: 4:30pm - 6:00pm | Room: Phoenix North

Moderator:

Marc Riedel - *Univ. of Minnesota, Twin Cities*

Organizers:

Bo Yuan - *City Univ. of New York*

Yanzhi Wang - *Syracuse Univ.*

Driven by the increasing demand in energy efficiency of computing system and the approaching limit of silicon device scaling, approximate computing has become a promising solution to design the next-generation energy-efficient computing system, especially for those inherently error-resilient applications, such as computer vision, signal processing, augmented reality etc. Among various types of approximate computing, stochastic computing, as a probabilistic theory-based computing technique, has very different information interpretation and processing style as compared to the other approximate computing techniques, thereby becoming a very unique category of the general approximate computing.

Based on its inherent low cost and error-resilience, to date stochastic computing has been successfully adopted in some commercial applications such as telecommunication. At the critical moment of we are experiencing both the gradual ending of Moore's law and the explosive increase of computation-intensive data-analysis applications, it is worthy to review and discuss the challenges and opportunities of stochastic computing. What can we learn from the history of stochastic computing? Will the emerging domain applications, such as deep learning, bring new opportunities of stochastic computing? What are the emerging impediments for stochastic computing in the big data era and what are the potential solutions? What methodology in the general approximate computing can help promote the future development of stochastic computing? There are many questions which need to be answered. In this panel, seven experts in the stochastic computing and general approximate computing community will provide their views on what the future looks like for stochastic computing. Audiences are welcome to participate in the discussion.

Panelists:

Kia Bazargan - *Univ. of Minnesota, Twin Cities*

Sunil Khatri - *Texas A&M Univ.*

Rajit Manohar - *Cornell Univ.*

Michael Orshansky - *Univ. of Texas at Austin*

Sherief Reda - *Brown Univ.*

Sachin Sapatnekar - *Univ. of Minnesota, Twin Cities*

Networking Reception

Time: 6:00pm - 6:30pm | Room: Phoenix Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

ACM/SIGDA Member Meeting

Time: 6:30pm - 8:00pm | Room: Phoenix Central

The annual ACM/SIGDA Member Meeting will be held on Tuesday evening from 6:30-8pm. The meeting is open for ACM SIGDA members to attend. Members of the Electronic Design Automation community who would like to learn more about SIGDA or get involved with SIGDA activities are also invited. Dinner and beverages will be served.

The meeting will begin with a brief overview of SIGDA, including its organization, activities, volunteering opportunities, and member benefits. We will then introduce this year's SIGDA Pioneering Achievement award recipient with an informal presentation on his life-long achievements. Next, the Outstanding Young Faculty Award winner will present a brief talk on his work. Finally, we will end the evening with the announcement of the winners of ACM Design Automation Student Research Competition taking place at this year's ICCAD. We hope to see you there!

Sponsored by:



Association for
Computing Machinery



Shuttle Information

ICCAD attendees can catch the shuttle to downtown Austin on Tuesday night from 6:00pm - 12:00am (Midnight). Service runs between the DoubleTree Hotel and the Driskill Hotel downtown.

Locations and Schedule:

Departing from the DoubleTree Hotel (In front of the hotel under the Porte Cochere):
6:00pm, 7:00pm, 8:00pm, 9:00pm, 10:00pm, 11:00pm

Departing from the Driskill Hotel downtown on the half hour:
6:30pm, 7:30pm, 8:30pm, 9:30pm, 10:30pm, 11:30pm

- WEDNESDAY SCHEDULE -

8:45 - 9:45am

Keynote: Learning and Multiagent Reasoning for Autonomous Robots

Room: Phoenix South

9:45 - 10:15am

Coffee Break

Room: Prefunction Foyer

10:15am - 12:15pm

Session 8A: Hardware-Assisted Solutions for Preventing Information Leakages

Room: Phoenix South

Session 8B: Challenges in Timing and Power Integrity

Room: Austin

Session 8C: Some Things Random, Wet, and Brainsy: Stochastic Computing, Microfluidics, and Neural Networks

Room: Robertson

Special Session 8D: Cross-Domain and Cross-Layer Techniques for Cyber-Physical System Security

Room: Phoenix North

12:30 - 1:30pm

Lunch

Room: Phoenix Central

1:45 - 3:45pm

Session 9A: Aging Analysis in Advanced Technologies

Room: Phoenix South

Session 9B: Design Techniques for Machine Learning

Room: Austin

Session 9C: Emerging Design Techniques for Non-volatile Memory and Logic

Room: Robertson

Session 9D: Why Power Matters: A Story of Thermals, Approximation and Mobile System Design

Room: Phoenix North

- WEDNESDAY SCHEDULE -

3:45 - 4:15pm

Coffee Break

Room: Prefunction Foyer

4:15 - 5:45pm

Session 10A: New Ideas In High-Level Synthesis

Room: Phoenix South

Session 10B: Reaching Out to the Third Dimension: New Floorplanning and Placement Techniques

Room: Austin

Embedded Tutorial 10C: From Biochips to Quantum Circuits: Computer-Aided Design for Emerging Technologies

Room: Robertson

Special Session 10D: Multilevel Design Understanding: From Specification to Logic

Room: Phoenix North

5:45 - 6:15pm

Networking Reception

Room: Phoenix Foyer



Keynote: Learning and Multiagent Reasoning for Autonomous Robots

Time: 8:45am - 9:45am | Room: Phoenix South

Speaker:

Peter Stone - *Univ. of Texas at Austin*

For robots to operate robustly in dynamic, uncertain environments, we are still in need of multidisciplinary research advances in many areas such as computer vision, tactile sensing, compliant motion, manipulation, locomotion, high-level decision-making, and many others. This talk will focus on two essential capabilities for robust autonomous intelligent robots, namely online learning from experience, and the ability to interact with other robots and with people. Examples of theoretically grounded research in these areas will be highlighted, as well as concrete applications in domains including robot soccer and autonomous driving.

Biography:

Dr. Peter Stone is the David Bruton, Jr. Centennial Professor of Computer Science at the University of Texas at Austin. In 2013 he was awarded the University of Texas System Regents' Outstanding Teaching Award and in 2014 he was inducted into the UT Austin Academy of Distinguished Teachers, earning him the title of University Distinguished Teaching Professor. Professor Stone's research interests in Artificial Intelligence include machine learning (especially reinforcement learning), multiagent systems, robotics, and e-commerce. He is an Alfred P. Sloan Research Fellow, Guggenheim Fellow, AAAI Fellow, Fulbright Scholar, and 2004 ONR Young Investigator. In 2003, he won an NSF CAREER award for his proposed long term research on learning agents in dynamic, collaborative, and adversarial multiagent environments, in 2007 he received the prestigious IJCAI Computers and Thought Award, given biannually to the top AI researcher under the age of 35, and in 2016 he was awarded the ACM/SIGAI Autonomous Agents Research Award.

8A - Hardware-Assisted Solutions for Preventing Information Leakage

Time: 10:15am - 12:15pm | Room: Phoenix South

Moderator:

Yiorgos Makris - *Univ. of Texas at Dallas*

The session presents hardware solutions for preventing information leakage through various side channels. Methodologies include tracking the information flow using hardware structures, adding extra permutation functions to protect symmetric block ciphers against differential power attacks, and leveraging the unique properties of emerging technologies to prevent machine learning attacks.

8A.1 A Hardware-based Technique for Efficient Implicit Information Flow Tracking

Jangseop Shin - *Seoul National Univ.*

Hongce Zhang - *Princeton Univ.*

Jinyong Lee, Ingoo Heo - *Seoul National Univ.*

Yu-Yuan Chen, Ruby Lee - *Princeton Univ.*

Yunheung Paek - *Seoul National Univ.*

8A.2 Imprecise Security: Quality and Complexity Tradeoffs for Hardware Information Flow Tracking

Wei Hu - *Univ. of California at San Diego*

Andrew Becker - *École Polytechnique Fédérale de Lausanne*

Armita Ardeshiricham - *Univ. of California at San Diego*

Yu Tai - *Northwestern Polytechnical Univ.*

Paolo Ienne - *École Polytechnique Fédérale de Lausanne*

Dejun Mu - *Northwestern Polytechnical Univ.*

Ryan Kastner - *Univ. of California at San Diego*

8A.3 Encasing Block Ciphers to Foil Key Recovery Attempts via Side Channel

Giovanni Agosta, **Alessandro Barengi**, Gerardo Pelosi, Michele Scandale
- *Politecnico di Milano*

8A.4 Security of Neuromorphic Computing: Thwarting Learning Attacks Using Memristor's Obsolescence Effect

Chaofei Yang, Beiye Liu - *Univ. of Pittsburgh*

Wujie Wen - *Florida International Univ.*

Mark Barnell, Qing Wu - *Air Force Research Lab*

Hai Li, Yiran Chen - *Univ. of Pittsburgh*

Jeyavijayan Rajendran - *Univ. of Texas at Dallas*

8B - Challenges in Timing and Power Integrity

Time: 10:15am - 12:15pm | Room: Austin

Moderator:

Albert Zeng - *Cadence Design Systems, Inc.*

Evolution of design and manufacturing technology necessitates further improvements in timing and power integrity analysis of modern designs. Performance of a design can be greatly affected by process variations and fluctuations of voltage. This session is dedicated to latest advances in variation-aware STA and IR-drop analysis. It starts with a paper describing improved statistical timing model for hierarchical SSTA. The second paper proposes use of GPU for a faster Monte Carlo simulation of a circuit under variations. The third paper demonstrates a way to reduce timing margin following a better modeling of hold-setup inter-dependency and the last paper proposes a method to speed up IR drop analysis.

8B.1 **Generation and Use of Statistical Timing Macro-models considering Slew and Load Variability**

Debjit Sinha, Vladimir Zolotov, Jin Hu, Sheshashayee Raghunathan, Adil Bhanji, Christine Casey - *IBM Corp.*

8B.2 **TinySPICE Plus: Scaling Up Statistical SPICE Simulations on GPU Leveraging Shared-Memory Based Sparse Matrix Solution Techniques**

Lengfei Han, Zhuo Feng - *Michigan Technological Univ.*

8B.3 **PieceTimer: A Holistic Timing Analysis Framework Considering Setup/Hold Time Interdependency Using A Piecewise Model**

Grace Li Zhang, Bing Li, Ulf Schlichtmann - *Technische Univ. München*

8B.4 **A Fast Layer Elimination Approach for Power Grid Reduction**

Abdul-Amir Yassine, Farid Najm - *Univ. of Toronto*



All speakers are denoted in bold | * denotes Best Paper Candidate

8C - Some Things Random, Wet, and Brainy: Stochastic Computing, Microfluidics, and Neural Networks

Time: 10:15am - 12:15pm | Room: Robertson

Moderator:

Tsung-Yi Ho - *National Tsing Hua Univ.*

This session consists of four presentation from three disparate, emerging areas in EDA: stochastic computing, microfluidics and neural networks. The first presentation revisits the topic of logical computation on stochastic bit streams and suggests that stochasticity is *not*, in fact, a requirement: stochastic computation can be made deterministic, with all the same benefits. The next two presentations discuss design challenges for two novel forms of microfluidics: paper-based systems and micro-electrode dot arrays. The final presentation discusses hyper-parameter optimization of neural networks. It suggest *using* neural networks to design neural networks.

8C.1 A Deterministic Approach to Stochastic Computation

Devon Jenson, Marc Riedel - *Univ. of Minnesota*

8C.2 Control-Fluidic CoDesign for Paper-Based Digital Microfluidic Biochips

Qin Wang, Zeyan Li - *Tsinghua Univ.*

Haena Cheong, Oh-Sun Kwon - *Sogang Univ.*

Hailong Yao - *Tsinghua Univ.*

Tsung-Yi Ho - *National Tsing Hua Univ.*

Kwanwoo Shin - *Sogang Univ.*

Bing Li, Ulf Schlichtmann - *Technische Univ. München*

Yici Cai - *Tsinghua Univ.*

8C.3 Neural Networks Designing Neural Networks: Multi-Objective Hyper-Parameter Optimization

Sean Smithson, Guang Yang, Warren Gross, Brett Meyer - *McGill Univ.*

8C.4 Error Recovery in a Micro-Electrode-Dot-Array Digital Microfluidic Biochip

Zipeng Li - *Duke Univ.*

Kelvin Yi-Tse Lai Lai, Po-Hsien Yu - *National Chiao Tung Univ.*

Krishnendu Chakrabarty, Miroslav Pajic - *Duke Univ.*

Tsung-Yi Ho - *National Tsing Hua Univ.*

Chen-Yi Lee - *National Chiao Tung Univ.*

Special Session 8D - Cross-Domain and Cross-Layer Techniques for Cyber-Physical System Security

Time: 10:15am - 12:15pm | Room: Phoenix North

Moderator:

Xin Li - *Carnegie Mellon Univ.*

Organizers:

Shiyan Hu - *Michigan Technological Univ.*

Yiyu Shi - *Univ. of Notre Dame*

Tremendous progress has been made in advancing Cyber-Physical System (CPS) technologies. We have explored foundational technologies that have spanned an ever-growing set of application domains, enabling breakthrough achievements in many of these fields. However, along with the rapid evolution of CPS technologies, it becomes imperative to address the security and reliability associated with them. The most effective and difficult to defend attacks are cross-domain and cross-layer attacks. Hackers do not launch attacks only based on hardware, software, or any single system. In contrast, those attacks are implemented in a cross-domain and cross-layer fashion, through exploring weak links in the connections among different systems in CPS. In this special session, four speakers will introduce the realistic security challenges in several critical CPS domains including smart home, emergency response, petroleum, and surveillance systems. They will demonstrate potential impacts of those attacks and how design automation can be explored to develop defense technologies for CPS security challenges.

8D.1 Privacy Protection via Appliance Scheduling in Smart Homes

Jie Wu, Jinglan Liu, Yiyu Shi, **X. Sharon Hu** - *Univ. of Notre Dame*

8D.2 Framework Designs to Enhance Reliable and Timely Services of Disaster Management Systems

Chi-Sheng Shih - *National Taiwan Univ.*

Pi-Cheng Hsiu - *Research Center for Information Technology Innovation, Academia Sinica, Taiwan*

Yuan-Hao Chang - *Institute of Information Science, Academia Sinica, Taiwan*

Shih-Hao Hung, Tei-Wei Kuo - *National Taiwan Univ.*

8D.3 Analysis of Production Data Manipulation Attacks in Petroleum Cyber-Physical Systems

Xiaodao Chen - *China University of Geosciences*

Yuchen Zhou - *Michigan Technological Univ.*

Hong Zhou, Chaowei Wan - *China University of Geosciences*

Qi Zhu - *Univ. of California, Riverside*

Wenchao Li - *Boston Univ.*

Shiyan Hu - *Michigan Technological Univ.*

8D.4 Security Challenges in Smart Surveillance Systems and the Solutions Based on Emerging Nano-devices

Chaofei Yang, Chunpeng Wu, **Yiran Chen**, Hai Li - *Univ. of Pittsburgh*

Qing Wu, Mark Barnell - *Air Force Research Lab*

Lunch

Time: 12:30pm - 1:30pm | Room: Phoenix Central

Join fellow attendees for lunch in Phoenix Central.

9A - Aging Analysis in Advanced Technologies

Time: 1:45pm - 3:45pm | Room: Phoenix South

Moderator:

Saurabh Sinha - *ARM, Inc.*

Aging mechanisms can seriously compromise the operation of devices and circuits. This session explores the latest physics and analysis techniques for interconnect and FinFET reliability. The first two papers present electromigration analysis for multi-branch wires, and the third paper improves the simulation efficiency with analytical models. The fourth paper explores reliability issues in FinFET devices. Such analysis subsequently enhances the reliability and quality of advanced IC design.

*9A.1 Fast Physics-Based Electromigration Checking for On-Die Power Grids

Sandeep Chatterjee - *Univ. of Toronto*

Valeriy Sukharev - *Mentor Graphics Corp.*

Farid N. Najm - *Univ. of Toronto*

9A.2 Exploring Aging Deceleration in FinFET-Based Multi-Core Systems

Ermao Cai, Dimitrios Stamoulis, Diana Marculescu - *Carnegie Mellon Univ.*

9A.3 An Efficient and Accurate Algorithm for Computing RC Current Response with Applications to EM Reliability Evaluation

Zhong Guan, Malgorzata Marek-Sadowska - *Univ. of California, Santa Barbara*

9A.4 Voltage-Based Electromigration Immortality Check for General Multi-Branch Interconnects

Zeyu Sun - *Univ. of California, Riverside*

Ertugrul Demircan, Mehul D. Shroff - *NXP Semiconductors*

Taeyoung Kim, Xin Huang, Sheldon Tan - *Univ. of California, Riverside*

9B - Design Techniques for Machine Learning

Time: 1:45pm - 3:45pm | Room: Austin

Moderator:

John Sartori - *Univ. of Minnesota*

This session introduces some new design methodologies for machine learning. The first paper proposes an efficient hardware implementation of the Johnson Lindenstrauss transform to operate on dimension-reduced data. The second paper proposes a robust and energy-efficient analog implementation of the spiking temporal encoder for brain-inspired computing system. The third paper introduces a method that uses machine learning to place process monitors for frequency prediction. The final paper presents a machine learning approach to locate the module in which a bug occurred.

9B.1 **Exploiting Randomness in Sketching for Efficient Hardware Implementation of Machine Learning Applications**

Ye Wang, Michael Orshansky, Constantine Caramanis - *Univ. of Texas at Austin*

9B.2 **Making neural encoding robust and energy-efficient: an advanced analog temporal encoder for brain-inspired computing systems**

Chenyuan Zhao, Jialing Li, **Yang Yi** - *Univ. of Kansas*

9B.3 **Statistical Methodology to Identify Optimal Placement of On-Chip Process Monitors for Predicting Fmax**

Szu-Pang Mu, Wen-Hsiang Chang - *National Chiao Tung Univ.*

Yi-Ming Wang, Ming-Tung Chang, Min-Hsiu Tsai - *Global Unichip Corp.*

Mango C.T. Chao - *National Chiao Tung Univ.*

9B.4 **BugMD: Automatic Mismatch Diagnosis for Bug Triaging**

Biruk Mammo, Milind Furia, Valeria Bertacco, Scott Mahlke - *Univ. of Michigan*
Daya Khudia - *Intel Corp.*



All speakers are denoted in bold | * denotes Best Paper Candidate

9C - Emerging Design Techniques for Non-volatile Memory and Logic

Time: 1:45pm - 3:45pm | Room: Robertson

Moderator:

Yiran Chen - *Univ. of Pittsburgh*

In this session, we consider non-volatile memory and logic technologies. The first paper presents a new magnetic memory structure that can store more than one bit of information per cell. The middle two papers consider more "coarse grained" logic-in-memory structures based on resistive RAM, while the last paper considers logic-in-memory at finer granularities via non-volatile ferroelectric FETs.

9C.1 **ODESY: a novel 3T-3MTJ cell design with Optimized area DENSITY, Scalability and latency**

Linuo Xue, Yuanqing Cheng - *Univ. of California, Santa Barbara*

Jianlei Yang - *Beihang Univ.*

Peiyuan Wang - *Qualcomm, Inc.*

Yuan Xie - *Univ. of California, Santa Barbara*

9C.2 **Delay-Optimal Technology Mapping for In-Memory Computing using ReRAM Devices**

Debjyoti Bhattacharjee, Anupam Chattopadhyay - *Nanyang Technological Univ.*

9C.3 **Reconfigurable In-Memory Computing with Resistive Memory Crossbar**

Yue Zha, Jing Li - *Univ. of Wisconsin*

9C.4 **Exploiting Ferroelectric FETs for Low-Power Non-Volatile Logic-in-Memory Circuits**

Xunzhao Yin - *Univ. of Notre Dame*

Ahmedullah Aziz - *Pennsylvania State Univ.*

Joseph Nahas - *Univ. of Notre Dame*

Sumeet Kumar Gupta - *Pennsylvania State Univ.*

Suman Datta, Michael Niemier, Xiaobo Sharon Hu - *Univ. of Notre Dame*



All speakers are denoted in bold | * denotes Best Paper Candidate

9D - Why Power Matters: A Story of Thermals, Approximation and Mobile System Design

Time: 1:45pm - 3:45pm | Room: Phoenix North

Moderator:

Jörg Henkel - *Karlsruhe Institute of Technology*

Power and thermal constraints are barriers for efficient system design. This session looks at the power and thermal management at various levels of granularity, starting from NoC to task scheduling and precision. The first paper deals with power and precision trade-offs. The second paper analyzes thermal effects in 3D ICs. NoC design for Near-Threshold computing is the focus of the third paper. The last paper in this session deals with power-efficient scheduling in mobile computing platforms.

9D.1 Approximation Knob: Power Capping Meets Energy Efficiency

Anil Kanduri, Mohammad-Hashem Haghbayan, Amir M. Rahmani, Pasi Liljeberg
- *Univ. of Turku*

Axel Jantsch - *Vienna Univ. of Technology*

Nikil Dutt - *Univ. of California, Irvine*

Hannu Tenhunen - *KTH Royal Institute of Technology*

9D.2 IC Thermal Analyzer for Versatile 3-D Structures Using Multigrid Preconditioned Krylov Methods

Scott Ladenheim, **Yi-Chung Chen**, Milan Mihajlovic, Vasilis Pavlidis - *Univ. of Manchester*

9D.3 BoostNoC: Power Efficient Network-on-Chip Architecture for Near Threshold Computing

Chidhambaranathan Rajamanikkam, Rajesh JayashankaraShrivedi, **Koushik Chakraborty**, Sanghamitra Roy - *Utah State Univ.*

9D.4 QScale: Thermally-Efficient QoS Management on Heterogeneous Mobile Platforms

Onur Sahin, Ayse K. Coskun - *Boston Univ.*

10A - New Ideas In High-Level Synthesis

Time: 4:15pm - 5:45pm | Room: Phoenix South

Moderator:

Hai (Helen) Li - *Univ. of Pittsburgh*

In this short session, we present three exciting papers in HLS. The first paper in this session automates the mapping of sequential programs to a network of hardware accelerators. The next paper deals with scheduling and data placement in a Coarse-grained Reconfigurable Array. Finally, the last paper presents a parallel implementation of graph queries in hardware.

10A.1 Synthesis of Statically Analyzable Accelerator Networks From Sequential Programs

Shaoyi Cheng, John Wawrzynek - *Univ. of California, Berkeley*

10A.2 Joint Loop Mapping and Data Placement for Coarse-Grained Reconfigurable Architecture with Multi-bank Memory

Shouyi Yin, **Xianqing Yao**, Tianyi Lu, Leibo Liu, Shaojun Wei - *Tsinghua Univ.*

10A.3 Efficient Synthesis of Graph Methods: a Dynamically Scheduled Architecture

Marco Minutoli, Vito Giovanni Castellana, Antonino Tumeo - *Pacific Northwest National Lab*
Marco Lattuada, Fabrizio Ferrandi - *Politecnico di Milano*

10B - Reaching Out to the Third Dimension: New Floorplanning and Placement Techniques

Time: 4:15pm - 5:45pm | Room: Austin

Moderator:

Evangeline Young - *Chinese Univ. of Hong Kong*

Monolithic 3D integration is a promising technology to improve wirelength, timing, and power consumption. The first paper in this session proposes a new partitioning and placement method that improves timing by mapping non-critical paths to the first tier of 3D integrated circuits (ICs) with slow tungsten metal layers. The second paper proposes a novel way to use existing 2D placement tools to create 3D ICs with solid performance. The third paper proposes a floorplanning technique that can incorporate diverse constraints and design choices into the 3D layout.

10B.1 Tier Partitioning Strategy to Mitigate BEOL Degradation and Cost Issues in Monolithic 3D ICs

Sandeep Kumar Samal - *Georgia Institute of Technology*

Deepak Nayak, Motoi Ichihashi, Srinivasa Banna - *GLOBALFOUNDRIES*

Sung Kyu Lim - *Georgia Institute of Technology*

10B.2 Cascade2D: A Design-Aware Partitioning Approach to Monolithic 3D IC with 2D Commercial Tools

Kyungwook Chang - *Georgia Institute of Technology*

Saurabh Sinha, Brian Cline, Raney Southerland, Michael Doherty, Greg Yeric - *ARM, Inc.*

Sung Kyu Lim - *Georgia Institute of Technology*

10B.3 SAINT: Handling Module Folding and Alignment in Fixed-outline Floorplans for 3D ICs

Jai-Ming Lin, Po-Yang Chiu, **Yen-Fu Chang** - *National Cheng Kung Univ.*

Embedded Tutorial 10C - From Biochips to Quantum Circuits: Computer-Aided Design for Emerging Technologies

Time: 4:15pm - 5:45pm | Room: Robertson

Moderator:

Rolf Drechsler - *Univ. of Bremen & DFKI GmbH*

Organizer:

Robert Wille - *Johannes Kepler Univ. of Linz*

While the previous decades have witnessed impressive developments in the design and realization of conventional computing devices, physical boundaries and cost restrictions led to an increasing interest in alternatives such as Quantum Computation, Optical Circuits, or Digital Microfluidic Biochips. Although most of these technologies are still in a rather “academic” state, first physical realizations have already been presented or even entered the market recently. This tutorial aims for providing an overview on the main concepts of selected emerging technologies as well as the resulting design methods. To this end, we review the respective physical as well as logical paradigms and introduce the correspondingly used circuit models. Based on that, we show how computer-aided design has to adapt the common tasks such as synthesis, optimization, verification, or technology mapping and review recently proposed solutions. An outlook to future challenges concludes the tutorial.

10C.1 From Biochips to Quantum Circuits: Computer-Aided Design for Emerging Technologies

Robert Wille - *Johannes Kepler Univ. of Linz*

Bing Li, **Ulf Schlichtmann** - *Technische Univ. München*

Rolf Drechsler - *Univ. of Bremen & DFKI GmbH*

Special Session 10D - Multilevel Design Understanding: From Specification to Logic

Time: 4:15pm - 5:45pm | Room: Phoenix North

Moderator:

Mark H. Ren - *NVIDIA Corporation*

Organizers:

Sandip Ray - *NXP Semiconductors*

Ian Harris - *Univ. of California, Irvine*

Goerschwin Fey - *Univ. of Bremen*

Mathias Soeken - *École Polytechnique Fédérale de Lausanne*

The design process is essentially a creative process which is reliant on the ability of designers to balance the interactions between a complex set of constraints to arrive at successful solutions. In order for designers to manage this task, they must collectively have a complete understanding of the behavior of the system, the mapping between behavior and structure, and the impact of each design feature on constraints such as power, performance, cost, and security. Design tasks require reasoning across multiple levels of abstraction in order to determine the impact of high-level design decisions, or to trace a design characteristic back to the feature which caused it. In a real design, cross-abstraction reasoning is difficult because the relationships between the different abstractions of a design are not captured. Designer time is expended discovering these cross-abstraction relationships in order to perform design, verification, and maintenance tasks. This special session will present the state-of-the-art in Design Understanding, research in approaches to provide designers with the design information needed in a concise and straightforward way. The volume of design information is enormous, so a significant part of the problem is determining what subset of information is relevant to the designer to assist with the particular design problem currently at hand.

10D.1 The Complexity of SoC Design Specifications

Sandip Ray - *NXP Semiconductors*

10D.2 Design Automation from Natural Language Specifications

Ian Harris - *Univ. of California, Irvine*

10D.3 Automatic Feature Localization in Hardware Designs

Goerschwin Fey - *Univ. of Bremen*

10D.4 Reverse Engineering Hardware Designs

Mathias Soeken - *EPFL Lausanne*

Networking Reception

Time: 5:45pm - 6:15pm | Room: Phoenix Foyer

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.

8:00am - 5:00pm

International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Room: Phoenix Central

Hardware and Algorithms for Learning On-a-chip (HALO)

Room: Phoenix North

Sponsored by:  

8:30am - 5:30pm

IEEE/ACM 9th Workshop on Variability Modeling and Characterization (VMC)

Room: Phoenix South

8:45am - 5:00pm

Workshop on Computer-Aided Design and Implementation for Cryptography and Security

Room: Austin



Save the Date for ICCAD 2017!

November 13 - 16, 2017

Location: Irvine Marriott, Irvine, CA



International Workshop on Design Automation for Analog and Mixed-Signal Circuits

Time: 8:00am - 5:00pm | Room: Phoenix Central

Organizers:

Xin Li - *Carnegie Mellon Univ.*

Zhuo Feng - *Michigan Technological Univ.*

Growing digitization of integrated circuits has contributed to making system-on-chips ever more complex. Yet, a substantial portion of a chip consists of analog and mixed-signal (AMS) circuits that provide critical functionality like signal conversion. Over the past several decades, aggressive scaling of IC technologies, as well as advancing the integration of heterogeneous physical domains on chip, substantially complicates the design of AMS components. On the one hand, their modeling and design becomes extremely complex. On the other hand, their interplay with the rest of the system-on-chip challenges design, verification and test. The new technology trends bring enormous challenges and opportunities for AMS design automation. This is reflected by an increase in research activity on AMS CAD worldwide. The purpose of this workshop is to bring together academic and industrial researchers from both design and CAD communities to report recent advances and motivate new research topics and directions in this area.

For more information, please visit: https://users.ece.cmu.edu/~xinli/2016_ams/

Speakers:

Yiran Chen - *Univ. of Pittsburgh*

Wei Wu - *Intel*

Peng Li - *Texas A&M Univ.*

Haralampos Stratigopoulos - *Laboratoire d'informatique de Paris 6*

Heidi Thornquist - *Sandia National Laboratories*

Ben Gu - *Cadence Design Systems, Inc.*

Chung-Kuan Cheng - *Univ. of California at San Diego*

Xin Li - *Carnegie Mellon Univ.*

Jun Tao - *Fudan Univ.*

Norihiro Kamae - *Kyoto Univ.*

Hardware and Algorithms for Learning On-a-chip (HALO)

Time: 8:00am - 5:00pm | Room: Phoenix North

Moderators:

Ganesh Dasika - ARM
Amit Trivedi - Univ. of Illinois
Sang Chin - Draper Lab

Organizers:

Yu Cao - Arizona State Univ.
Xin Li - Carnegie Mellon Univ.
Jae-sun Seo - Arizona State Univ.

Machine learning algorithms, such as those for image based search, face recognition, multi-category classification, and scene analysis, are being developed that will fundamentally alter the way individuals and organizations live, work, and interact with each other. However their computational complexity still challenges the state-of-the-art computing platforms, especially when the application of interest is tightly constrained by the requirements of low power, high throughput, small latency, etc. Examples include Internet of Things (IoT), autonomous vehicles, smart drones, and intelligent robots. In recent years, there have been enormous advances in implementing machine learning algorithms with application-specific hardware (e.g., FPGA, ASIC, etc.). There is a timely need to map the latest learning algorithms to physical hardware, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness. Recent progress in computational neurosciences and nanoelectronic technology, such as resistive memory devices, will further help shed light on future hardware-software platforms for learning on-a-chip.

For more information, please visit: <http://nimo.asu.edu/halo>

Speakers:

Rob A. Rutenbar - Univ. of Illinois
Eriko Nurvitadhi - Intel
Yu Wang - Tsinghua Univ.
Vivienne Sze - Massachusetts Institute of Technology
Andrew Howard - Google, Inc.
Huafeng Yu - Boeing
Yu Cheng - IBM
Asim Roy - Arizona State Univ.
Catherine D. Schuman - Oak Ridge National Laboratory
Kaushik Roy - Purdue Univ.
Thiago Mosqueiro - University of California at San Diego

Sponsored by:



IEEE/ACM 9th Workshop on Variability Modeling and Characterization (VMC)

Time: 8:30am - 5:30pm | Room: Phoenix South

Organizers:

Rasit Topaloglu - *IBM Corp.*

Takashi Sato - *Kyoto Univ.*

Duane Boning - *Massachusetts Institute of Technology*

This workshop provides a forum to discuss current practice as well as near future research needs of variability/reliability and their impact on design performance and cost. Furthermore, technical aspects of variability/reliability characterization, compact modeling, statistical simulation, test structure design, CAD, and resilient design are also covered. This workshop provides an opportunity to discuss modeling and characterization needs in emerging devices, semiconductor manufacturing technology, and computing schemes. We strive to establish links among technology, device physics, device models, EDA tools, related circuit and system design necessities. Please visit <http://www.cerc.utexas.edu/utda/vmc/> for Call for Papers and up to date information.

Speakers:

Kaushik Roy - *Purdue Univ.*

Henry Smith - *Massachusetts Institute of Technology & LumArray, Inc.*

Zhihong Chen - *Purdue Univ.*

Masanori Hashimoto - *Osaka Univ.*

Lei He - *Univ. of California, Los Angeles*

Kafai Lai - *IBM Research*

Hayden Taylor - *Univ. of California, Berkeley*

Takashi Tokuda - *Nara Institute of Science and Technology*

Workshop on Computer-Aided Design and Implementation for Cryptography and Security

Time: 8:45am - 5:00pm | Room: Austin

Organizers:

François Dupressoir - *University of Surrey*

Tim Güneysu - *Univ. of Bremen & DFKI GmbH*

Apostol Vassilev - *National Institute of Standards and Technology*

The Workshop on Computer-Aided Design and Implementation for Cryptography and Security (CADICS) aims at providing a platform for the discussion of computer-aided security, from secure hardware design to secure software implementation and to secure system integration. The workshop aims at federating recent efforts in developing computer-aided techniques in these individual communities and at promoting dialogue and collaboration across their boundaries, supporting the development of computer-aided design techniques and tools for the construction, implementation and deployment of secure systems. Affiliation with ICCAD will particularly foster exchanges with the broader electronic design community, providing a platform for the exchange of ideas at the intersection of formal methods, security and hardware design, with a special focus on constructing a unified view of the security-relevant properties that can be guaranteed by hardware designers and the hardware assumptions made when reasoning about software security.

For more details on the workshop's program and agenda, please visit the workshop webpage: <http://informatik.uni-bremen.de/CADICS>

Speakers:

Mohit Tiwari - *Univ. of Texas at Austin*

Stephen Trimberger - *Xilinx Inc.*

Patrick Schaumont - *Virginia Tech*

- EXECUTIVE COMMITTEE -



GENERAL CHAIR

Frank Liu
IBM Research Austin
11501 Burnet Rd.
MS 904-6G017
Austin, TX 78758
512-286-7267
frankliu@us.ibm.com



PAST CHAIR

Diana Marculescu
Carnegie Mellon Univ.
Dept. of Electrical and
Computer Engineering
5000 Forbes Ave.
Pittsburgh, PA 15213
412-268-1167
dianam@cmu.edu



PROGRAM CHAIR

Sri Parameswaran
Univ. of New South Wales
School of Computer Science
& Engineering
Sydney, Australia
61296626725
sridevan@cse.unsw.edu.au



VICE PROGRAM CHAIR

Iris Bahar
School of Engineering
Brown University
182 Hope Street
Providence, RI 02906
401-863-1430 (office)
401-603-6972 (mobile)
iris_bahar@brown.edu



TUTORIAL & SPECIAL SESSION CHAIR

David Z. Pan
Dept. of Electrical &
Computer Engineering
The Univ. of Texas at Austin City
Austin, TX 78712
512-471-1436
dpan@ece.utexas.edu



WORKSHOP CHAIR

Rolf Drechsler
University of Bremen/DFKI
Bibliothekstr. 1, 28359, Bremen,
Germany
+49 421 218 63932
drechsle@
informatik.uni-bremen.de



EUROPEAN REPRESENTATIVE

Lars Hedrich
University of Frankfurt
Dept. of Computer Science
& Mathematics
60325 Frankfurt, Germany
+49 (0)69-798-22297
hedrich@em.cs.uni-frankfurt.de



ASIAN REPRESENTATIVE

Shih-Chieh Chang
National Tsing Hua University
Dept. of Computer Science
Hsin-Chu, Taiwan, R.O.C.
scchang@cs.nthu.edu.tw



ACM/SIGDA REPRESENTATIVE

Yuan Xie
University of California, Santa Barbara
5159 HFH Hall, UCSB
Santa Barbara, CA 93106
805-893-5563
yuanxie@ece.ucsb.edu



CEDA REPRESENTATIVE

Gi-Joon Nam
IBM T.J. Watson Research Center
1101 Kitchawan Rd
Yorktown Heights, NY 10598
512-286-7713
gnam@us.ibm.com



CONFERENCE PLANNER & REGISTRATION MANAGER

Nannette Jordan
MP Associates, Inc.
1721 Boxelder St., Ste. 107
Louisville, CO 80027
303-530-4562
Nannette@mpassociates.com

- TECHNICAL PROGRAM COMMITTEE -

PROGRAM CHAIR

Sri Parameswaran
*Univ. of New South Wales, School of
Computer Science & Engineering*

Mohammad Al Faruque
Univ. of California, Irvine

Jose Ayala
Univ. Complutense De Madrid

Lars Bauer
Karlsruhe Institute of Technology

Duane Boning
*Massachusetts Institute of
Technology*

Philip Brisk
Univ. of California, Riverside

Arquimedes Canedo
Siemens Corp.

Yu (Kevin) Cao
Arizona State Univ.

Aiqun Cao
Synopsys, Inc.

Noureddine Chabini
Royal Military College of Canada

Koushik Chakraborty
Utah State Univ.

Hung-Ming Chen
National Chiao Tung Univ.

Chen-Mou Cheng
National Taiwan Univ.

Kiyoung Choi
Seoul National Univ.

Jordi Cortadella
Univ. Politècnica de Catalunya

Masoud Daneshtalab
KTH Royal Institute of Technology

Sabya Das
Xilinx, Inc.

Azadeh Davoodi
Univ. of Wisconsin

Jennifer Dworak
Southern Methodist Univ.

VICE PROGRAM CHAIR

Iris Bahar
School of Engineering, Brown University

Wolfgang Ecker
Infineon Technologies AG

Abe Elfadel
*Masdar Institute of Science and
Technology*

Shao-Yun Fang
*National Taiwan Univ. of Science
and Technology*

Yunsi Fei
Northeastern Univ.

Zhuo Feng
Michigan Technological Univ.

Farshad Firouzi
IMEC/Katholieke Univ. Leuven

Domenic Forte
Univ. of Florida

Swaroop Ghosh
Pennsylvania State Univ.

Dip Goswami
Eindhoven Univ. of Technology

Daniel Grosse
Univ. of Bremen

Jie Gu
Northwestern Univ.

Puneet Gupta
Univ. of California, Los Angeles

Sandeep Gupta
Univ. of Southern California

Ian Harris
Univ. of California, Irvine

Masanori Hashimoto
Osaka Univ.

Stephan Held
Univ. of Bonn

Ahmed Hemani
KTH Royal Institute of Technology

Jörg Henkel
Karlsruhe Institute of Technology

Christian Hochberger
Technische Univ. Darmstadt

Shiyan Hu
Michigan Technological Univ.

Jiang Hu
Texas A&M Univ.

Shih-Hao Hung
National Taiwan Univ.

Hsiao-Chun Hung
National Taiwan Univ.

Haris Javaid
Google, Inc.

Timothy Kam
Intel Corp.

Ulya Karpuzcu
Univ. of Minnesota

Ramesh Karri
New York Univ.

Chandramouli Kashyap
Intel Corp.

Ryan Kastner
Univ. of California at San Diego

Eric Keiter
Sandia National Laboratories

Igor Keller
Cadence Design Systems, Inc.

Sunil Khatri
Texas A&M Univ.

Taemin Kim
Intel Corp.

Victor Kravets
IBM Research

Smita Krishnaswamy
Columbia Univ.

Eren Kursun
Columbia Univ.

- TECHNICAL PROGRAM COMMITTEE -

Xiaolue Lai

Cadence Design Systems, Inc.

Peter Langendörfer

IHP Microelectronics

Jongeeun Lee

*Ulsan National Institute of
Science and Technology (UNIST)*

Jing Li

Univ. of Wisconsin, Madison

Ruiming Li

Oracle Corp.

Hai (Helen) Li

Univ. of Pittsburgh

Bing Li

Technische Univ. München

Xin Li

Carnegie Mellon Univ.

Yun (Eric) Liang

Peking Univ.

Sung Kyu Lim

Georgia Institute of Technology

Guojie Luo

Peking Univ.

Yiorgos Makris

Univ. of Texas at Dallas

Michail Maniatakos

New York Univ. Abu Dhabi

Dmitri Maslov

National Science Foundation

Gayatri Mehta

Univ. of North Texas

Natasia Miskov-Zivanov

Univ. of Pittsburgh

Anca Molnos

CEA-LETI

Nicola Nicolici

McMaster Univ.

Michael Niemier

Univ. of Notre Dame

Umit Ogras

Arizona State Univ.

Miroslav Pajic

Duke Univ.

Partha Pande

Washington State Univ.

Sangyoung Park

Technische Univ. München

Srinivas Patil

Qualcomm Technologies, Inc.

Gerardo Pelosi

Politecnico di Milano

Gang Qu

Univ. of Maryland

Wenjing Rao

Univ. of Illinois at Chicago

Sayak Ray

Intel Corp.

Sherief Reda

Brown Univ.

Francesco Regazzoni

AlaRI

Marc Riedel

Univ. of Minnesota

Janet Roveda

Univ. of Arizona

Ramesh S.

General Motors R&D

Marco Santambrogio

Politecnico di Milano

John Sartori

Univ. of Minnesota

Ulf Schlichtmann

Technische Univ. München

Dimitrios Serpanos

*Univ. of Patras & Qatar
Computing Research Institute*

Cristina Silvano

Politecnico di Milano

Sebastian Steinhorst

Technische Univ. München

Yasuhiro Takashima

Univ. of Kitakyushu

Natarajan Viswanathan

Cadence Design Systems, Inc.

Pascal Vivet

CEA-LETI

Yu Wang

Tsinghua Univ.

Chun-Yao Wang

National Tsing Hua Univ.

Jia Wang

Illinois Institute of Technology

Georg Weissenbacher

Vienna Univ. of Technology

Kai-Chiang Wu

National Chiao Tung Univ.

Yuan Xie

Univ. of California, Santa Barbara

Sungjoo Yoo

Seoul National Univ.

Takahide Yoshikawa

Fujitsu Laboratories Ltd.

Bei Yu

Chinese Univ. of Hong Kong

Wenjian Yu

Tsinghua Univ.

Huafeng Yu

Boeing Research & Technology

Haibo Zeng

*Virginia Polytechnic Institute and
State Univ.*

Zhiyu Zeng

Cadence Design Systems, Inc.

Zhiru Zhang

Cornell Univ.

Wei Zhang

*Hong Kong Univ. of Science and
Technology*

Zheng Zhang

*Massachusetts Institute of
Technology*

Youtao Zhang

Univ. of Pittsburgh

Pingqiang Zhou

ShanghaiTech Univ.

- CONFERENCE SPONSORS -



Association for
Computing Machinery

About ACM

ACM, the Association for Computing Machinery, acm.org, is the world's largest educational and scientific computing society, uniting computing educators, researchers and professionals to inspire dialogue, share resources and address the field's challenges. ACM strengthens the computing profession's collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence.

ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. ACM provides the computing field's premier Digital Library (DL), an invaluable online resource of over two million fully searchable pages of text, including a 50+ year archive, from ACM's high quality journals and proceedings. The DL also reaches the entire world of computing through the fully integrated Guide to Computing Literature. ACM's 37 Special Interest Groups (SIGs) focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as SIGGRAPH, SPLASH including OOPSLA, DAC, ICCAD and CHI, giving members opportunities to meet experts in their fields of interest and network with other knowledgeable members.

Become an ACM member today and join thousands of other leading professionals, researchers and academics who benefit from all ACM has to offer. Join ACM online at acm.org, or contact ACM directly by phone: 800-342-6626 (US and Canada) or 212-626-0500 (Global), by fax: 212-944-1318, or by e-mail: acmhelp@acm.org.



Join ACM/SIGDA: The Resource For EDA Professionals

ACM/SIGDA, (Special Interest Group on Design Automation) provides a broad array of resources to our members, to students, professors, industry professionals and, to the EDA field in general. SIGDA sponsors various events to promote interaction among the community to share the latest technical and professional advances. It also serves as a forum to support events that nurture new ideas and infuse vitality into new emerging trends in the field.

SIGDA has a long history of supporting conferences and the EDA profession including ICCAD, DAC, DATE, and ASP-DAC, plus around 15 focused symposia and workshops. SIGDA supports various events such as - the University Research Demonstration that helps to foster interactions between students and industry; Design Automation Summer School that exposes students to trending topics; Young Faculty Workshops; Ph.D. Forums in conjunction with major conferences, design contests such as CAD Athlon. SIGDA funds various scholarships and recognizes outstanding research publications. Awards recognize significant contributions at all stages of the professional career from student awards to the Pioneer Award for Lifetime achievement. SIGDA has launched new programs such as SIGDA Live, a series of monthly webinars on topics of general interest to the SIGDA community and a more global E-Newsletter with a newly formed editorial board. SIGDA also supports local chapters that help with professional networking. SIGDA also administrates Student Research Competition on behalf of ACM.

SIGDA pioneered electronic publishing of EDA literature, beginning with the DA Library in 1989. SIGDA also provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems). Major benefits provided to SIGDA members include free access to all SIGDA sponsored publications in the ACM Digital Library, and reduced registration rates for SIGDA sponsored events.

For further information on SIGDA's programs and resources, see sigda.org.

Please join us in building a more vibrant community and volunteer for SIGDA.

- CONFERENCE SPONSORS -



IEEE IEEE

IEEE is the world's largest professional association dedicated to advancing technological innovation and excellence for the benefit of humanity. IEEE and its members inspire a global community through IEEE's highly cited publications, conferences, technology standards, and professional and educational activities.



IEEE Council on Electronic Design Automation (CEDA)

The IEEE Council on Electronic Design Automation (CEDA) provides a focal point for EDA activities spread across six IEEE societies (Antennas and Propagation, Circuits and Systems, Computer, Electron Devices, Microwave Theory and Techniques, and Solid-State Circuits). The Council sponsors or co-sponsors over a dozen key EDA conferences including: the Design Automation Conference (DAC), Asia and South Pacific Design Automation Conference (ASP-DAC), International Conference on Computer Aided Design (ICCAD), Design Automation and Test in Europe (DATE), and events at Embedded Systems Week (ESWeek). The Council also publishes IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems (TCAD), IEEE Design & Test (D&T), and IEEE Embedded Systems Letters (ESL). In order to promote the recognition of leading EDA professionals, the Council sponsors the A. Richard Newton, Phil Kaufman, Ernest S. Kuh Early Career, TCAD Donald O. Pederson Best Paper, and William J. McCalla ICCAD Best Paper Awards. The Council welcomes new volunteers and local chapters.

For more information on CEDA, visit: iee-ceda.org.



CAS

The IEEE Circuits and Systems Society's field of interest spans the theory, analysis, design (computer aided design), and practical implementation of circuits, and the application of circuit theoretic techniques to systems and to signal processing. The coverage of this field includes the spectrum of activities from, and including, basic scientific theory to industrial applications.

The IEEE Circuits and Systems Society (CASS) believes that the Grand Engineering Challenges of the 21st century can only be addressed in an inter-disciplinary and cross-disciplinary manner. The Society's unique and profound expertise in Circuits, Systems, Signals, Modeling, Analysis, and Design can have a decisive impact on important issues such as Sustainable Energy, Bio-Health, Green Information Technology, Nano-Technology, and Scalable Information Technology Systems.

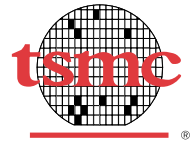
Our mission is to foster CASS members across disciplines to address humanity's grand challenges by conceiving and pioneering solutions to fundamental and applied problems in circuits and systems.



IEEE Electron Devices Society

The IEEE Electron Devices Society (EDS) is involved in the advancement of electronics and electrical engineering through research, development, design, manufacture, materials, and applications of electron devices. EDS is concerned with technical, educational, scientific publication and meeting activities which provide benefits to members while contributing towards the progress of this field. eds.ieee.org.

*Thank You to our Technical Program Dinner
Corporate Sponsors ...*



cadence®

BUILD THE NEXT INNOVATIVE PRODUCT

From chips to boards to system



Cadence technologies help you create unique products that transform lives.

- Custom and analog design
- Digital design
- Enterprise verification
- System development and verification
- Package and PCB design, plus signal and power integrity analysis
- Processor, memory, interface, and verification IP

Learn more at www.cadence.com



NOVEMBER 7-10, 2016 • AUSTIN, TX • ICCAD.COM