

FINAL PROGRAM

*The premier conference for
Electronic Design Technology*
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*November 2-5, 2009
DoubleTree Hotel
San Jose, CA*

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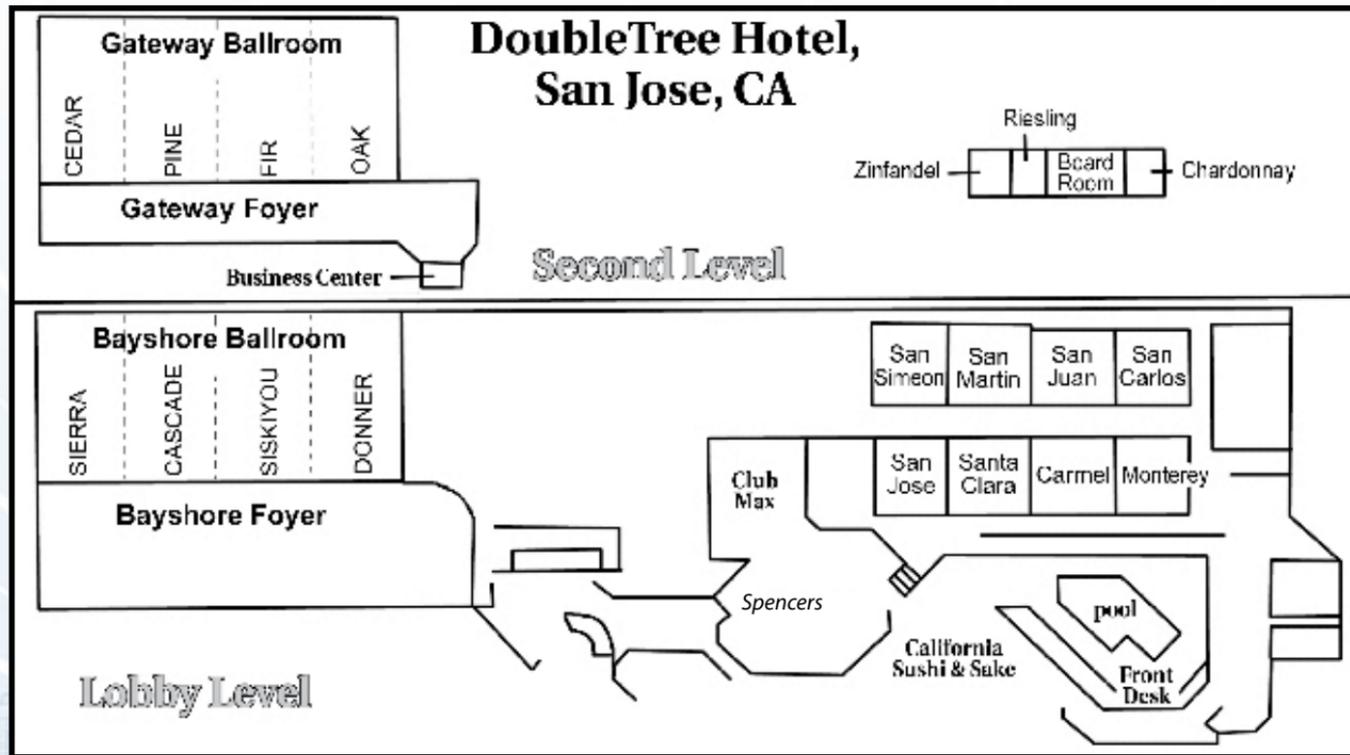
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Table of Contents

Welcome Message.....	Inside Front Cover
Hotel Map.....	2
Best Paper Candidates/Committee	3
CADathlon at ICCAD	4
Technology Fair	5 - 6
Monday - Wednesday Session Matrix.....	7 - 9
Opening Session/Awards.....	10
Monday Keynote Address.....	11
Monday Sessions.....	12 - 19
Monday Panel	20
ACM/SIGDA Member Meeting.....	21
Meetings at ICCAD.....	22
Tuesday Sessions.....	23 - 34
Tuesday Lunch Talk.....	28
Wednesday Sessions.....	35 - 39
Thursday Colocated Workshops	40 - 41
Executive Committee	43
Program Committee	44 - 45
Conference Sponsors.....	46 - 48
General Info/ICCAD Archive.....	Inside Back Cover





Best Paper Candidates/Award Committee

Best Paper Award Committee

Louis Scheffer
Janelia Farms Research Campus
Howard Hughes Medical Institute
Ashburn, VA

Joel Phillips
Cadence Research Labs
Berkeley, CA

Abhijit Davare
Intel Corp.
Hillsboro, OR

Patrick Groeneveld
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Karam Chatha
Arizona State Univ.
Tempe, AZ

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

Monday Sessions

- 1D.1 SCHEDULING WITH SOFT CONSTRAINTS**
Jason Cong, Bin Liu - *Univ. of California, Los Angeles*
Zhiru Zhang - *AutoESL Design Technologies, Inc.*
- 2B.1 IN-PLACE RECONFIGURATION FOR FPGA FAULT TOLERANCE**
Zhe Feng, Yu Hu, Lei He, Rupak Majumdar - *Univ. of California, Los Angeles*
- 2C.1 SAT-BASED PROTEIN DESIGN**
Noah Ollikainen - *Univ. of California, San Francisco*
Ellen Sentovich - *Consultant*
Carlos Coelho - *Cadence Design Systems, Inc.*
Tanja Kortemme - *Univ. of California, San Francisco*
Andreas Kuehlmann - *Cadence Design Systems, Inc.*
- 3A.1 PRE-BOND TESTABLE LOW-POWER CLOCK TREE DESIGN FOR 3-D STACKED ICs**
Xin Zhao, Dean L. Lewis, Hsien-Hsin S. Lee, Sung Kyu Lim - *Georgia Institute of Technology*
- 3C.1 EXACT ROUTE MATCHING ALGORITHMS FOR ANALOG AND MIXED SIGNAL INTEGRATED CIRCUITS**
Mustafa Ozdal, Renato Hentschke - *Intel Corp.*
- 3D.1 THERMAL MODELING FOR 3-D-ICs WITH INTEGRATED MICROCHANNEL COOLING**
Hitoshi Mizunuma, Chia-Lin Yang, Yi-Chang Lu - *National Taiwan Univ.*

Tuesday Sessions

- 4B.1 THE EPSILON-APPROXIMATION TO DISCRETE VT ASSIGNMENT FOR LEAKAGE POWER MINIMIZATION**
Yujia Feng, Shiyan Hu - *Michigan Technological Univ.*
- 4C.1 TAPE: THERMAL-AWARE AGENT-BASED POWER ECONOMY FOR MULTI/MANY-CORE ARCHITECTURES**
Thomas Ebi, Mohammad Abdullah Al Faruque, Jörg Henkel - *Univ. Karlsruhe*
- 5A.1 A HIERARCHY OF SUBGRAPHS UNDERLYING A TIMING GRAPH AND ITS USE IN CAPTURING TOPOLOGICAL CORRELATION IN SSTA**
Jaeyong Chung, Jacob A. Abraham - *Univ. of Texas, Austin*
- 5C.1 THE SYNTHESIS OF COMBINATIONAL LOGIC TO GENERATE PROBABILITIES**
Weikang Qian, Marc D. Riedel, Kia Bazargan, David J. Lilja - *Univ. of Minnesota*
- 7A.1 AN ELEGANT HARDWARE-CORROBORATED STATISTICAL REPAIR AND TEST METHODOLOGY FOR CONQUERING AGING EFFECTS**
Rouwaida Kanj, Rajiv Joshi, Chad Adams, James Warnock, Sani Nassif - *IBM Corp.*
- 7C.1 FROM 2-D TO 3-D NOCS: A CASE STUDY ON WORST-CASE COMMUNICATION PERFORMANCE**
Yue Qian - *National Univ. of Defense Technology*
Zhonghai Lu - *Royal Institute of Technology*
Wenhua Dou - *National Univ. of Defense Technology*

Wednesday Sessions

- 8C.1 VOLTAGE-DROP AWARE ANALYTICAL PLACEMENT BY GLOBAL POWER SPREADING FOR MIXED-SIZE CIRCUIT DESIGNS**
Yi-Lin Chuang, Po-Wei Lee, Yao-Wen Chang - *National Taiwan Univ.*
- 9B.2 A HIERARCHICAL FLOATING RANDOM WALK ALGORITHM FOR FABRIC-AWARE 3-D CAPACITANCE EXTRACTION**
Tarek A. El-Moselhy - *Massachusetts Institute of Technology*
Ibrahim M. Elfadel - *IBM Corp.*
Luca Daniel - *Massachusetts Institute of Technology*



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The CADathlon at ICCAD

ACM/SIGDA sponsors the eighth annual EDA programming contest at ICCAD

Sunday, November 1, 7:30am - 5:00pm Donner Ballroom

The CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork.

In its eighth year as the "Olympic games of EDA," the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field.

The contest is open to two-person teams of graduate students specializing in CAD and currently full-time enrolled in a Ph.D. granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Travel grants are provided to qualifying students.

The CADathlon competition consists of six problems in the following areas:

- (1) Circuit Design & Analysis
- (2) Physical Design
- (3) Logic & High-Level Synthesis
- (4) System Design & Analysis
- (5) Functional Verification
- (6) Bio-EDA

More specific information about the problems and relevant research papers will be released on the internet one week prior to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges' test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given. The team that earns the highest score is declared the winner. In addition to handsome trophies, the first place team's prize is a \$2,000 cash award. The second place team's prize is a \$1,000 cash award.

Contest winners will be announced at the ICCAD Opening Session on Monday morning and celebrated at the ACM/SIGDA Member Meeting on Monday evening.

The CADathlon competition is sponsored by ACM/SIGDA, Denali, Synopsis, Intel, SRC, Atrenta and ARM. For detailed contest information and sample problems from last year's competition, please visit the ACM/SIGDA website at <http://www.sigda.org/programs/cadathlon>.

Or contact members of the **CADathlon organizing committee**:

- Chair, Asst. Prof. Matthew Guthaus, mrg@soe.ucsc.edu
- Finance Chair, Asst. Prof. Sudeep Pasricha, sudeep.pasricha@gmail.com
- Publicity Chair, Assoc. Prof. Srinivas Katkoori, katkoori@cse.usf.edu
- Registration Chair, Asst. Prof. Qing Wu, qwu@binghamton.edu
- Website Chair, Jarrod Roy, royj@eecs.umich.edu



Technology Fair

Library Technologies

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Exhibiting ChipTimer, Timing Closure Tool, starting with gate level netlist, 10% fewer gates, and as much as 30% better timing without new cells, and as much as 2X better performance with additional new cells, works both pre- and post-layout; SolutionWare, Cell, IO and Memory Characterization-Modeling with distributed and multi-core support; CellOpt, timing and power Optimizer for cells, adders and multipliers, generates low power cells with user controlled timing characteristics; YieldOpt, one step wc/bc corner model generator under process variation, for each cell in a library, with predictable probabilities for critical paths and timing analysis under user control. Eliminates the need for SSTA.

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Si2 (Silicon Integration Initiative, Inc.)

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Austin, TX 78759
512-342-2244
www.si2.org

Si2 (Silicon Integration Initiative) is the largest organization of industry-leading semiconductor, systems, EDA and manufacturing companies focused on the development and adoption of standards to improve the way integrated circuits are designed and manufactured, in order to speed time-to market, reduce costs, and meet the challenges of sub-micron design. Now in its 21st year, Si2 is uniquely positioned to enable timely collaboration through dedicated staff and a strong implementation focus driven by its member companies. Si2 represents nearly 100 companies involved in all parts of the silicon supply chain throughout the world. See www.si2.org.

Gateway Foyer
Monday, November 2, 10:00am - 6:00pm



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Technology Fair

Springer

233 Spring St.
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Springer is one of the world-leaders in Engineering book publishing, boasting a broad range of subject matter, and a history of working with the most prestigious scholars in the field. Additionally, Springer publishes an astute collection of Journals, with a track record of generating the latest sought after content. Visit our booth to purchase our latest publications at a 20% conference discount. Our publishers are available to answer any questions you may have. Visit springer.com for more information on our latest products.

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Stone Pillar Technologies is the leading provider of software tools supporting semiconductor process technology development. Our products automate the creation of parametric test chips, and enable the creation of complete test plans through simple drag-and-drop operations. Test results produced in this way are automatically linked to details such as wafer and die location, test conditions, device geometries and structure layout to facilitate comprehensive data analysis. Stone Pillar Suite saves our customers engineering time and capital, and improves traceability and technology development processes, reducing the engineering cost of test chip and test plan creation by as much as 90%.

Gateway Foyer
Monday, November 2, 10:00am - 6:00pm

Monday, November 2, 2009

Registration - 7:30am - 6:30pm
 Technology Fair - 10:00am - 6:00pm
 Speakers' Breakfast - 7:30am

(Bayshore Foyer)
 (Gateway Foyer)
 (Siskiyou Ballroom)

9:00 AM TO 10:30 PM **General Session & Award Presentation**
Keynote Address: *Impact of Cloud Computing on Extreme Scale Analytics Platforms, Hamid Pirahesh, IBM/ACM Fellow, San Jose, CA* (Oak/Fir Ballroom)

Break: 10:30 - 11:00am

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom	Donner Ballroom
11:00 AM TO 12:30 PM	Session 1A <i>Functional Verification</i>	Session 1B <i>Advances in Routing</i>	Session 1C <i>Tutorial: Design for Manufacturability: Current Practice and Future Directions</i>	Session 1D <i>Scheduling Techniques for Low Power</i>	Session 1E <i>Special Session: Resilient Computing</i>

Lunch: 12:30 - 1:30pm (Siskiyou Ballroom)

Technology Fair Dessert Reception: 1:30 - 2:00pm

2:00 PM TO 4:00 PM	Session 2A <i>Advances in Test Efficiency</i>	Session 2B <i>Advances in FPGA Synthesis and Trustable Silicon</i>	Session 2C <i>Design Automation for Biological Systems</i>	Session 2D <i>Analysis and Mitigation of Transient and Permanent Failures</i>	Session 2E <i>Tutorial: An Introduction to Satisfiability Modulo Theories</i>
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Break: 4:00 - 4:30pm

4:30 PM TO 6:00 PM	Session 3A <i>Emerging Topics in Test and Reliability</i>	Session 3B <i>Timing Closure and Design Robustness</i>	Session 3C <i>Routing in Alternative Technologies</i>	Session 3D <i>Emerging Design and Memory Technologies</i>	Session 3E <i>Tutorial: Embedded Processors, Methods and Applications: Computer Architects Perspective</i>
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Reception: 6:00 - 6:30pm

6:30 PM TO 7:30 PM **Panel: The Future of Engineering Publication (Fir Ballroom)**

7:30 PM TO 9:30 PM **ACM/SIGDA Member Meeting (Siskiyou Ballroom)**

Tuesday, November 3, 2009

Registration - 7:30am - 6:00pm (Bayshore Foyer)
Speakers' Breakfast - 7:30am (Siskiyou Ballroom)

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom	Donner Ballroom
8:30 AM TO 10:00 AM	Session 4A Tutorial: Introduction to GPU Programming for EDA	Session 4B Analytical Advances in Physical Synthesis	Session 4C Thermal-Aware Management Techniques for Multi-Core Architectures	Designer Track: When SPICE is not Enough	Session 4E Tutorial: Analysis and Testing of Concurrent Programs
Coffee Break: 10:00 - 10:30am					
10:30 AM TO 12:00 PM	Session 5A Statistical Timing Analysis and Its Application	Session 5B Congestion Driven Placement	Session 5C New Applications in Logic Synthesis	Designer Track: Practical Experience and Future Tool Directions at New Process Nodes	
Lunch Presentation: Smart Grid for the 21st Century: 12:00 - 1:15pm (Siskiyou Ballroom)					Sponsored By:  
1:30 PM TO 3:30 PM	Session 6A Advanced Modeling and Simulation Methods	Session 6B Characterization and Compensation of Variability	Session 6C Policies and Methods for Low Power	Session 6D Emerging Memory Technologies	Session 6E Special Session: Power 7 - Verification Challenges of a High-End 8-Core Microprocessor
Coffee Break: 3:30 - 4:00pm					
4:00 PM TO 6:00 PM	Session 7A Advanced Device Reliability and Modeling	Session 7B Clock Optimization and Parallel Algorithm in EDA	Session 7C Analysis and Optimization of Network-On-Chip and Multiprocessor SOC	Session 7D Design-Patterning Interactions	Session 7E Special Session: Statistical Timing: Where is the Tofu?
ICCAD Reception: 6:00 - 8:00pm (Siskiyou Ballroom)					

Wednesday, November 4, 2009

Registration - 7:30am - 1:00pm (Bayshore Foyer)
Speakers' Breakfast - 7:30am (Siskiyou Ballroom)

	Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom	Donner Ballroom
8:30 AM TO 10:00 AM	Session 8A <i>Yield Estimation and Optimization for SRAMs</i>	Session 8B <i>Thermal Modeling and Analysis at Chip and Platform Levels</i>	Session 8C <i>Analytic Placement</i>	Session 8D <i>Performance and Power Issues in Embedded System-Level Design</i>	Session 8E <i>Tutorial: Biological Circuits and Systems</i>
Coffee Break: 10:00 - 10:30am					
10:30 AM TO 12:00 PM	Session 9A <i>Statistical Simulation and Optimization of Serial Link and Wordlength</i>	Session 9B <i>Parasitic Extraction, Modeling, and Reduction Techniques</i>	Session 9C <i>Advanced Boolean Techniques in Logic Synthesis</i>	Session 9D <i>Tutorial: Global Routing Revisited</i>	
Lunch: 12:30 - 1:30pm (Siskiyou Ballroom)					



Opening Session

9:00 - 10:30am • Oak/Fir Ballroom

Opening Remarks

Jaijeet Roychowdhury - **General Chair** - Univ. of California, Berkeley

Award Presentations

IEEE/ACM William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

TAPE: Thermal-Aware Agent-Based Power Economy for Multi/Many-Core Architectures

Thomas Ebi, Mohammad Abdullah Al Faruque, Jörg Henkel - Univ. Karlsruhe

An Elegant Hardware-Corroborated Statistical Repair and Test Methodology for Conquering Aging Effects

Rouwaida Kanj, Rajiv Joshi, Chad Adams, James Warnock, Sani Nassif - IBM Corp.

2008 IEEE Transactions on Computer-Aided Design Donald O. Pederson Best Paper Award

Using Simulation and Satisfiability to Compute Flexibilities in Boolean Networks

Authors: **Mishchenko, A., Zhang, J., Sinha, S., Burch, R., Brayton, R., Chrzanowska-Jeske, M.**

Vol. 25, no. 5, pp. 743-755, May 2006

IEEE CEDA Early Career Award

Igor Markov - Univ. of Michigan

For outstanding contributions to algorithms, methodologies, and software for the physical design of integrated circuits.

2009 SIGDA Pioneering Achievement Award

Martin Davis - New York Univ.

For contributions to algorithms for solving the Boolean Satisfiability problem, which heavily influenced modern tools for hardware and software verification, as well as logic circuit synthesis.

Keynote Address

9:00 - 10:30am • Monday, November 2 • Oak/Fir Ballroom



Impact of Cloud Computing on Extreme Scale Analytics Platforms

Hamid Pirahesh, IBM/ACM Fellow

Information technology is going through a fundamental change, influenced primarily by (1) Flexible provisioning and scalability of Cloud Computing, (2) Accelerated pace of analytics around semi-structured and unstructured data in the context of semantically rich data objects in the main stream data processing, (3) Much increased human interaction with the web due to the use of GPS enabled mobile devices, and its application in our daily lives, from social networking to conducting financial transactions, (4) Web Scale programming community with Web 2.0, search and open software, (5) Rise of SaaS (Software As A Service).

There is particular emphasis on breaking the complexity barrier of today's solutions through simplification. The lifetime cost of ownership of solutions is dominated by the human time spent in building, operating, and evolving these solutions. Much increased compute power in cloud computing enables us to reduce this complexity by reducing the use of fragile, complex, and partially manually optimized programs in favor of simpler and more stable and scalable ones. Flexibility and much quicker provisioning of cloud computing combined with much reduced cost per terra byte/flop are key factors in much faster deployment of solutions.

High scale cloud platforms play an increasingly bigger role in the strategy of NSF and other government agencies. IBM-google cloud is an example of an effort that provides cloud services for universities. Societal smarter planet applications, such as Smart Traffic, energy grids, healthcare, cities are increasingly important for both government and commercial companies. Commercially viable high scale compute and storage infrastructure is a key enabler for these applications. As such, in the context of the data intensive applications, there are significant opportunities in optimizing multicore chips and hardware/storage systems.

Hamid Pirahesh, Ph.D., is an IBM fellow, ACM Fellow and is a senior manager responsible for the exploratory database research department at IBM Almaden Research Center. Pirahesh is an IBM master inventor, and is a member of IBM Academy. He is a core member of IBM Information Management Architecture board, and has direct responsibilities in various aspects of IBM information management products, including IBM DB2 product.

Time: 11:00 AM - 11:00 AM

Room: Oak

SESSION 1A**Functional Verification

Moderators: Andreas Kuehlmann - *Cadence Design Systems, Inc.*
Sanjit A. Seshia - *Univ. of California, Berkeley*

Satisfiability solvers are key components of functional verification tools. This session includes three papers on the design and application of satisfiability solvers in functional verification. The first paper applies satisfiability modulo theories (SMT) solvers to the verification of analog circuits. The second paper proposes a technique to more efficiently generate interpolants in Boolean satisfiability (SAT) solving. The final paper presents a new decision procedure for a subset of finite-precision bit-vector arithmetic.

- 1A.1 First Steps Towards SAT-Based Formal Analog Verification
Saurabh Tiwary (stiwary@cadence.com), Anubhav Gupta, Joel Phillips, Claudio Pinello, Radu Zlatanovici - *Cadence Design Systems, Inc.*
- 1A.2 Interpolant Generation without Constructing Resolution Graph
Chih-Jen Hsu, Shao-Lun Huang, Chi-An Wu, **Chung-Yang (Ric) Huang** (ric@cc.ee.ntu.edu.tw) - *National Taiwan Univ.*
- 1A.3 A Scalable Decision Procedure for Fixed-Width Bit-Vectors
Roberto Bruttomesso (roberto.bruttomesso@unisi.ch), Natasha Sharagina - *Univ. della Svizzera Italiana*

Time: 11:00 AM - 12:30 PM

Room: Fir

SESSION 1B • ADVANCES IN ROUTING

Moderators: Ting-Chi Wang - *National Tsing-Hua Univ.*
Chris Chu - *Iowa State Univ.*

This session focuses on practical routing problems. The first two papers deal with the basic obstacle-avoiding rectilinear Steiner minimum tree problem. The third paper considers both shorts and opens for redundant wire insertion. Finally, a power-switch chain routing algorithm for multi-threshold CMOS designs is proposed in the last paper.

- 1B.1 **GENERATION OF OPTIMAL OBSTACLE-AVOIDING RECTILINEAR STEINER MINIMUM TREE**
Liang Li, Zaichen Qian, **Evangeline F.Y. Young** (fyyoung@cse.cuhk.edu.hk) - *The Chinese Univ. of Hong Kong*
- 1B.2 **OBSTACLE-AVOIDING RECTILINEAR STEINER TREE CONSTRUCTION BASED ON STEINER POINT SELECTION**
Chih-Hung Liu - *National Taiwan Univ.*
Shih-Yi Yuan - *Feng Chia Univ.*
Sy-Yen Kuo, **Jung-Hung Weng** (r97943148@ntu.edu.tw) - *National Taiwan Univ.*
- 1B.3S **HOW TO CONSIDER SHORTS AND GUARANTEE YIELD RATE IMPROVEMENT FOR REDUNDANT WIRE INSERTION**
Fong-Yuan Chang (FongYuan.Chang@gmail.com), Ren-Song Tsay, Wai-Kei Mak - *National Tsing-Hua Univ.*
- 1B.4S **POWER-SWITCH ROUTING FOR COARSE-GRAIN MTCMOS TECHNOLOGIES**
Tsun-Ming Tseng (ted2060@gmail.com), Mango C.-T. Chao - *National Chiao-Tung Univ.*
Chien-Pang Lu, Chen-Hsing Lo - *Mstar Semiconductor*

Time: 11:00 AM - 12:30 PM

Room: Pine

SESSION 1C • TUTORIAL: DESIGN FOR MANUFACTURABILITY: CURRENT PRACTICE AND FUTURE DIRECTIONS

Moderator: Michael Orshansky - *Univ. of Texas, Austin*
Organizers: Lou Scheffer - *Janelia Farms, Howard Hughes Medical Institute*
Yao-Wen Chang - *National Taiwan Univ.*

1C.1 DESIGN FOR MANUFACTURABILITY FOR THE 45nm TECHNOLOGY AND BEYOND Charles Chiang, Jamil Kawa - *Synopsys, Inc.*

At the time our book was published two and a half years ago, the 45nm technology node was well established and the 32nm, 28nm, and 22 nm were in various stages of introduction and development. The discussion over the need for high "k" dielectric to suppress leakage at advanced nodes was settled, but not so was the debate over issues such as the need for double patterning and for what layers need that, the production readiness of EUV and its implications for what course of lithography will be pursued for each node, the future of planar bulk CMOS versus the use of FINFETS versus the emergence of other structures and techniques.

Also, the research into controlling intra-die variability never slowed down. In this talk we will update you on DFM technology in light of the progress made on the above mentioned issues. The talk will start with an industrial mask synthesis flow from CMP to Mask Data Preparation (MDP) and/or Mask Error Check (MRC). Then it will cover feature scale CMP modeling and timing modeling that take CMP into account. On lithography the talk will introduce and cover the progress in the two new technologies: the Double Patterning Technology (DPT) and Extreme Ultraviolet (EUV) Technology.

1C.2 E-BEAM DIRECT WRITE AND DESIGN FOR E-BEAM Aki Fujimura - *D2S, Inc.*

Mask-based lithography solutions are becoming more sophisticated in writing features that are a fraction of the wavelength of light being used to write them. The amazing set of innovations allow the leading-edge node to continue with Moore's Law. But mask costs and depth of focus, particularly for contacts and double patterning, are increasing the economic barrier for the leading-edge technology nodes.

The higher the barrier, the smaller the number of design starts, which is unhealthy for the entire semiconductor supply chain.

Maskless direct-writing of wafers offers a healthy alternative path for the industry, particularly for low-volume, high-value designs, and for contact layers. Overall, the tutorial will enable you to gain a better understanding for the maskless e-beam direct write technologies in production today, as well as a glimpse into the roadmap for the future.

Time: 11:00 AM - 12:30 PM

Room: Cedar

SESSION 1D • SCHEDULING TECHNIQUES FOR LOW POWER

Moderator: Ahmed M. Eltawil - *Univ. of California, Irvine*

The papers in this session develop new scheduling techniques to address IC power consumption and reliability issues. The first paper presents a new scheduling algorithm for high-level synthesis with soft timing constraints. The second paper develops a new customized instruction set for run-time energy minimization. The third paper develops a system-level scheduling algorithm to optimize system reliability while minimizing area overhead.

1D.1 B SCHEDULING WITH SOFT CONSTRAINTS

Jason Cong, **Bin Liu** (bliu@cs.ucla.edu) - *Univ. of California, Los Angeles*
Zhuru Zhang - *AutoESL Design Technologies, Inc.*

1D.2 REMIS: RUN-TIME ENERGY MINIMIZATION SCHEME IN A RECONFIGURABLE PROCESSOR WITH DYNAMIC POWER-GATED INSTRUCTION SET

Muhammad Shafique (shafique@ira.uka.de), Lars Bauer, Jörg Henkel - *Univ. Karlsruhe*

1D.3 ENHANCED RELIABILITY-AWARE POWER MANAGEMENT THROUGH SHARED RECOVERY TECHNIQUE

Baoxian Zhao (bzhao@gmu.edu), Hakan Aydin - *George Mason Univ.*
Dakai Zhu - *Univ. of Texas, San Antonio*

Time: 11:00 AM - 12:30 PM

Room: Donner

SPECIAL SESSION 1E • RESILIENT COMPUTING

Moderator: Sandeep Gupta - *Univ. of Southern California*
Organizer: Massoud Pedram - *Univ. of Southern California*

Computing systems have become integral to all aspects of our lives, including manufacturing, construction, transportation, health-care, education, finance, and so on. Hence, even short-lived interruptions of critical computing resources will cause severe societal disruptions. This is making resilient computing an increasing concern in all domains and at every level - chip, server, data-center, and global interconnected computing and communication infrastructure. As the concern for resilience has become universal and extended well beyond the confines of handful of high-end application domains - such as aerospace and mainframes of financial firms - it has become increasingly imperative to develop approaches for improving resilience that consider tradeoffs between resilience, energy, performance, and total system cost.

This session will focus on three perspectives on resilience. The first speaker will present an overview of decades of academic research on this subject. The second speaker will describe the research and development trajectory in a systems company that has been considering resilience for many decades. The last speaker will describe how resilience considerations are shaping the development of microprocessor chips in ways that were unimaginable a decade ago.

1E.1 RESILIENCE IN COMPUTER SYSTEMS AND NETWORKS

Kishor Trivedi (kst@ee.duke.edu), Dong Seong Kim, Rahul Ghosh - *Duke Univ.*

1E.2 THE BULLET-PROOF MAINFRAME: AN INDUSTRY PERSPECTIVE ON RESILIENT SYSTEM DESIGN

Charles Webb (cfw@us.ibm.com) - *IBM Corp.*

1E.3 RESILIENT CIRCUITS - ENABLING ENERGY-EFFICIENT PERFORMANCE AND RELIABILITY

James Tschanz (james.w.tschanz@intel.com), Keith Bowman, Chris Wilkerson, Shih-Lien Lu, Tanay Karnik - *Intel Corp.*

All speakers are denoted in bold
S - denotes short paper
B - denotes best paper candidate

Monday, November 2, 2009

Time: 2:00 PM - 4:00 PM

Room: Oak

SESSION 2A • ADVANCES IN TEST EFFICIENCY

Moderator: Yiorgos Makris - *Yale Univ.*

The first paper introduces an advanced linear algebra method for selecting goals that minimize power consumption during scan-based test. The second paper leverages logic implication checkers used for concurrent error detection in order to eliminate superfluous test vectors. The third paper employs a novel path selection algorithm for alleviating the problem of process space coverage loss due to unsensitizable paths. The last paper presents a multi-part solution to reduce IR drop in circuits with combinational decompressors.

2A.1 SCAN POWER REDUCTION IN LINEAR TEST DATA COMPRESSION SCHEME

Mingjing Chen, **Alex Orailoglu** (alex@cs.ucsd.edu) - *Univ. of California, San Diego*

2A.2 COMPACTING TEST VECTOR SETS VIA STRATEGIC USE OF IMPLICATIONS

Nuno Alves (nuno@brown.edu) - *Brown Univ.*
Kundan Nepal - *Bucknell Univ.*
Jennifer Dworak, R. Iris Bahar - *Brown Univ.*

2A.3 PRE-ATPG PATH SELECTION FOR NEAR OPTIMAL POST-ATPG PROCESS SPACE COVERAGE

Jinjun Xiong (jinjun@us.ibm.com) - *IBM Corp.*
Yiyu Shi - *Univ. of California, Los Angeles*
Vladimir Zolotov, Chandu Visweswariah - *IBM Corp.*

2A.4 A NOVEL POST-ATPG IR-DROP REDUCTION SCHEME FOR AT-SPEED SCAN TESTING IN BROADCAST-SCAN-BASED TEST COMPRESSION ENVIRONMENT

Kohei Miyase (k_miyase@cse.kyutech.ac.jp), Yuta Yamato - *Kyushu Institute of Technology*
Kenji Noda, Hideaki Ito, Kazumi Hatayama, Takashi Aikyo - *STARC*
Xiaoqing Wen, Seiji Kajihara - *Kyushu Institute of Technology*

Time: 2:00 PM - 4:00 PM

Room: Fir

SESSION 2B • ADVANCES IN FPGA SYNTHESIS AND TRUSTABLE SILICON

Moderators: Sherief Reda - *Brown Univ.*
Ilya Ganusov - *Achronix Semiconductor Corp.*

This session presents new advances in FPGA synthesis and verification techniques for trustable silicon. The first paper proposes a new logic re-synthesis algorithm that leads to improved fault-tolerant designs, while the second paper proposes a novel memory structure that improves the energy-delay product of FPGA-based designs. The last three papers offer new methods for Trojan detection. The third paper proposes to use design obfuscation methods to neutralize Trojan insertion techniques. The fourth and fifth papers propose methods that detect Trojans using novel power analysis techniques.

2B.1 B IN-PLACE RECONFIGURATION FOR FPGA FAULT TOLERANCE

Zhe Feng (feng07@ucla.edu), Yu Hu, Lei He, Rupak Majumdar - *Univ. of California, Los Angeles*

2B.2 A CIRCUIT-SOFTWARE CO-DESIGN APPROACH FOR IMPROVING EDP IN RECONFIGURABLE FRAMEWORKS

Swarup Bhunia, **Somnath Paul** (sxp190@case.edu) - *Case Western Reserve Univ.*
Saibal Mukhopadhyay, Subho Chatterjee - *Georgia Institute of Technology*

2B.3 SECURITY AGAINST HARDWARE TROJAN THROUGH A NOVEL APPLICATION OF DESIGN OBFUSCATION

Swarup Bhunia, **Rajat Subhra Chakraborty** (rschakraborty@gmail.com) - *Case Western Reserve Univ.*

2B.4S MOLES: MALICIOUS OFF-CHIP LEAKAGE ENABLED BY SIDE-CHANNELS

Christof Paar - *Univ. Bochum*
Lang Lin (llin@ecs.umass.edu), Wayne Burseson - *Univ. of Massachusetts, Amherst*

2B.5S CONSISTENCY-BASED CHARACTERIZATION FOR IC TROJAN DETECTION

Yousra Alkabani (yousra@rice.edu), Farinaz Koushanfar - *Rice Univ.*

Time: 2:00 PM - 4:00 PM

Room: Pine

SESSION 2C • DESIGN AUTOMATION FOR BIOLOGICAL SYSTEMS

Moderator: Chris Myers - *Univ. of Utah*

This session presents emerging ideas in design automation for biological systems. The first paper presents SAT formulation to minimize energy of a given protein structure. The second paper introduces compilation strategy and tool kit to perform sequential arithmetic computation on protein quantities. The third paper presents an algorithm for identifying thermodynamically-favored metabolic pathways. The fourth paper discusses an approach that reduces routing complexity in digital microfluidic biochips.

2C.1 B SAT-BASED PROTEIN DESIGN

Noah Ollikainen (nollikai@gmail.com) - *Univ. of California, San Francisco*
Ellen Sentovich - *Consultant*
Carlos Coelho - *Cadence Design Systems, Inc.*
Tanja Kortemme - *Univ. of California, San Francisco*
Andreas Kuehlmann - *Cadence Design Systems, Inc.*

2C.2 SYNTHESIZING SEQUENTIAL REGISTER-BASED COMPUTATION WITH BIOCHEMISTRY

Adam Shea, Brian Fett, **Marc Riedel** (mriedel@umn.edu), Keshab Parhi - *Univ. of Minnesota*

2C.3 A WEIGHTED GRAPH ALGORITHM FOR IDENTIFYING DOMINANT-EDGE METABOLIC PATHWAYS

Ehsan Ullah, Kyongbum Lee, **Soha Hassoun** (soha@cs.tufts.edu) - *Tufts Univ.*

2C.4 A CONTAMINATION AWARE DROPLET ROUTING ALGORITHM FOR DIGITAL MICROFLUIDIC BIOCHIPS

Tsung-Wei Huang (tyho@mail.ncku.edu.tw), Chun-Hsien Lin, Tsung-Yi Ho - *National Cheng Kung Univ.*

Time: 2:00 PM - 4:00 PM

Room: Cedar

SESSION 2D • ANALYSIS AND MITIGATION OF TRANSIENT AND PERMANENT FAILURES

Moderators: Jörg Henkel - *Univ. Karlsruhe*
Ahmed M. Eltawil - *Univ. of California, Irvine*

This session presents papers that address reliability concerns due to soft errors, aging, timing errors and variation. The first paper proposes a statistical soft error rate analysis framework. The second paper presents a statistical tuning methodology to mitigate the aging impact on pipeline structures. The third paper proposes a new optimization technique for timing speculation based on the dynamic behavior of the circuit. The final paper in the session proposes to map critical data to memory areas that are less likely to fail in order to improve Quality of Service and yield under presence of process variations.

2D.1 ON SOFT ERROR RATE ANALYSIS OF SCALED CMOS DESIGNS - A STATISTICAL PERSPECTIVE

Huan-Kai Peng (pumbaapeng@gmail.com), Charles H.-P. Wen - *National Chiao-Tung Univ.*
Jayanta Bhadra - *Freescale Semiconductors, Inc.*

2D.2 INTRINSIC NBTI-VARIABILITY AWARE STATISTICAL PIPELINE PERFORMANCE ASSESSMENT AND TUNING

Balaji Vaidyanathan (vbalaji@tsmc.com) - *Pennsylvania State Univ. and Taiwan Semiconductor Manufacturing Co., Ltd.*
Anthony Oates - *Taiwan Semiconductor Manufacturing Co., Ltd.*
Yuan Xie - *Pennsylvania State Univ.*

2D.3 DYNATUNE: CIRCUIT-LEVEL OPTIMIZATION FOR TIMING SPECULATION CONSIDERING DYNAMIC PATH BEHAVIOR

Lu Wan (luwan2@illinois.edu), Deming Chen - *Univ. of Illinois, Urbana-Champaign*

2D.4 A VARIATION-AWARE PREFERENTIAL DESIGN APPROACH FOR MEMORY BASED RECONFIGURABLE COMPUTING

Somnath Paul (appusom@gmail.com) - *Case Western Reserve Univ.*
Saibal Mukhopadhyay - *Georgia Institute of Technology*
Swarup Bhunia - *Case Western Reserve Univ.*

Time: 2:00 PM - 4:00 PM

Room: Donner

SESSION 2E • TUTORIAL: AN INTRODUCTION TO SATISFIABILITY MODULO THEORIES

Formal verification and testing of circuits and software increasingly rely on satisfiability solvers for logics more expressive than propositional logic. This tutorial will focus on Satisfiability Modulo Theories (SMT): determining satisfiability of first-order formulas with respect to one or more background theories. Tremendous progress has been made in SMT in recent years, and SMT solvers are being used in an increasing number of applications.

The tutorial will start with a review of useful background theories such as equality with uninterpreted function, arrays, linear arithmetic, and finite-precision bit-vectors. Some representative applications will also be briefly surveyed.

The tutorial will mainly focus on the major techniques for SMT solving, including the so-called lazy and eager approaches. The lazy approach, also referred to as DP(L)T, involves combining specialized solvers for the background theories with a Boolean satisfiability (SAT) solver; we will describe both the mechanisms for combining theories as well as the techniques required for combining Boolean and theory-based reasoning. The eager approach involves performing optimized theory-specific encodings to SAT; specific topics include small-domain encodings and rewrite-based techniques.

Finally, we will briefly mention some extensions to the basic framework, including abstraction-based methods, proof generation, quantifier instantiation, and interpolant generation. Our goal in this tutorial is to introduce the ICCAD audience to the fundamentals of SMT to enable them to extend and adapt SMT solvers to applications such as word-level equivalence checking, model checking, analysis and testing of embedded software, system-level design, and techniques for the analysis of analog and mixed-signal designs.

Presenters: **Clark Barrett** - *New York Univ.*
Sanjit A. Seshia - *Univ. of California, Berkeley*

Time: 4:30 PM - 6:00 PM

Room: Oak

SESSION 3A • EMERGING TOPICS IN TEST AND RELIABILITY

Moderator: Jim Plusquellic - *Univ. of New Mexico*

The first two papers address the test challenges associated with pre-bond 3-D dies. The third paper proposes a method for optimizing the allocation of BIST controllers to multiple embedded memory cores. The last paper introduces a synergy between reliability monitoring resources and the operating system to avoid performance degradation.

3A.1 B PRE-BOND TESTABLE LOW-POWER CLOCK TREE DESIGN FOR 3-D STACKED ICs

Xin Zhao (xinzha@ece.gatech.edu), Dean L. Lewis, Hsien-Hsin S. Lee, Sung Kyu Lim - *Georgia Institute of Technology*

3A.2 LAYOUT-DRIVEN TEST-ARCHITECTURE DESIGN AND OPTIMIZATION FOR 3-D SOCS UNDER PRE-BOND TEST-PIN-COUNT CONSTRAINT

Li Jiang (lijiang@cse.cuhk.edu.hk), Qiang Xu - *The Chinese Univ. of Hong Kong*
Krishnendu Chakrabarty - *Duke Univ.*
T. M. Mak - *Intel Corp.*

3A.3S BIST DESIGN OPTIMIZATION FOR LARGE-SCALE EMBEDDED MEMORY CORES

Tzuo-Fan Chien (hoolank@eda.ee.ntu.edu.tw), Wen-Chi Chao, Chien-Mo Li, Yao-Wen Chang, Kuan-Yu Liao - *National Taiwan Univ.*
Ming-Tung Chang, Min-Hsiu Tsai, Chih-Mou Tseng - *Global Unichip Corp.*

3A.4S OPERATING SYSTEM SCHEDULING FOR EFFICIENT ONLINE SELF-TEST IN ROBUST SYSTEMS

Yanjing Li (yanjingl@stanford.edu) - *Stanford Univ.*
Onur Mutlu - *Carnegie Mellon Univ.*
Subhasish Mitra - *Stanford Univ.*

Time: 4:30 PM - 6:00 PM

Room: Fir

SESSION 3B • TIMING CLOSURE AND DESIGN ROBUSTNESS

Moderators: Chirayu S. Amin - *Intel Corp.*
Igor Keller - *Cadence Design Systems, Inc.*

This session focuses on methods of pessimism reduction in timing analysis and improving robustness of design to process variations. The first paper proposes a metric to quantify design robustness to parameter variations. The second paper utilizes parameterized STA to drive post-silicon design optimization. Authors of the last paper in this session propose an efficient method of false pessimism reduction in noise-on-delay analysis.

- 3B.1 QUANTIFYING ROBUSTNESS METRICS IN PARAMETERIZED STATIC TIMING ANALYSIS**
Khaled R. Heloue (khaled@eecg.utoronto.ca) - *Univ. of Toronto*
Chandramouli V. Kashyap - *Intel Corp.*
Farid N. Najm - *Univ. of Toronto*
- 3B.2 PSTA-BASED BRANCH AND BOUND APPROACH TO THE SILICON SPEEDPATH ISOLATION PROBLEM**
Sari Onaissi (sari@eecg.utoronto.ca), Khaled R. Heloue, Farid N. Najm - *Univ. of Toronto*
- 3B.3 TIMING ARC BASED LOGIC ANALYSIS FOR FALSE NOISE REDUCTION**
Murthy Palla (Murthy.Palla@gmail.com), Jens Bargfrede - *Infineon Technologies AG*
Stephan Eggersgluess, Walter Anheier, Rolf Drechsler - *Univ. Bremen*

Time: 4:30 PM - 6:00 PM

Room: Pine

SESSION 3C • ROUTING IN ALTERNATIVE TECHNOLOGIES

Moderators: Dwight Hill - *Synopsys, Inc.*
Cheng-Kok Koh - *Purdue Univ.*

These four papers explore problems and solutions beyond the classical digital IC routing domain.

- 3C.1 B EXACT ROUTE MATCHING ALGORITHMS FOR ANALOG AND MIXED SIGNAL INTEGRATED CIRCUITS**
Mustafa Ozdal (mustafa.ozdal@intel.com), Renato Hentschke - *Intel Corp.*
- 3C.2 AN EFFICIENT PRE-ASSIGNMENT ROUTING ALGORITHM FOR FLIP-CHIP DESIGNS**
Po-Wei Lee (webber@eda.ee.ntu.edu.tw), Chung-Wei Lin, Yao-Wen Chang - *National Taiwan Univ.*
Chin-Fang Shen, Wen-Chih Tseng - *Synopsys, Inc.*
- 3C.3S OPTIMAL LAYER ASSIGNMENT FOR ESCAPE ROUTING OF BUSES**
Tan Yan (tanyan2@illinois.edu), Hui Kong, Martin D. F. Wong - *Univ. of Illinois, Urbana-Champaign*
- 3C.4S PAD ASSIGNMENT FOR DIE-STACKING SYSTEM-IN-PACKAGE DESIGN**
Yu-Chen Lin, **Wai-Kei Mak** (wkmak@cs.nthu.edu.tw) - *National Tsing-Hua Univ.*
Chris Chu - *Iowa State Univ.*
Ting-Chi Wang - *National Tsing-Hua Univ.*

Time: 4:30 PM - 6:00 PM

Room: Cedar

SESSION 3D • EMERGING DESIGN AND MEMORY TECHNOLOGIES

Moderators: Deming Chen - *Univ. of Illinois, Urbana-Champaign*
Aman Gayasen - *Achronix Semiconductor Corp.*

The session presents advances in 3-D thermal modeling, STT-RAM Energy reduction and Phase Change Memory simulation. The first paper proposes an ultra-fast thermal model for 3-D-ICs with microchannel cooling system. The second paper utilizes early write termination to reduce energy consumed by STT-RAMs. The final paper presents a Phase Change RAM simulator to enable architectural-level explorations of power and performance.

3D.1 B THERMAL MODELING FOR 3-D-ICs WITH INTEGRATED MICROCHANNEL COOLING

Hitoshi Mizunuma (hitoshi_mizunuma@tet.toshiba.co.jp), Chia-Lin Yang, Yi-Chang Lu - *National Taiwan Univ.*

3D.2 ENERGY REDUCTION FOR STT-RAM USING EARLY WRITE TERMINATION

Ping Zhou (piz7@pitt.edu), Bo Zhao, Jun Yang, Youtao Zhang - *Univ. of Pittsburgh*

3D.3 PCRAMSIM: SYSTEM-LEVEL PERFORMANCE, ENERGY, AND AREA MODELING FOR PHASE-CHANGE RAM

Xiangyu Dong (xydong@cse.psu.edu) - *Pennsylvania State Univ.*
Norm Jouppi - *Hewlett-Packard Co.*
Yuan Xie - *Pennsylvania State Univ.*

Time: 4:30 PM - 6:00 PM

Room: Donner

SESSION 3E • TUTORIAL: EMBEDDED PROCESSORS, METHODS AND APPLICATIONS: COMPUTER ARCHITECTS PERSPECTIVE

As feature sizes diminish and transistors multiply, designers are compelled to move to higher levels of abstraction to overcome the productivity gap. Increasingly designers use processors as the main module in embedded system design. The available choices to the modern designer include processor (which are both non-configurable and configurable), DSP and GPU cores. This tutorial explores the available processors, details methodologies and explains applications.

The tutorial is divided into three parts: the first will explore the field of embedded processors; the second will look design methodologies based on embedded processors; the third, will describe an application in detail. This tutorial will be presented by three experienced researchers with industrial and academic experience, and will benefit students, researchers, and design engineers.

Presenters: **Grant Martin** - *Tensilica, Inc.*
Sri Parameswaran - *Univ. of New South Wales*
Anand Raghunathan - *Purdue Univ.*

PANEL • THE FUTURE OF ENGINEERING PUBLICATION

Moderator: Joel Phillips - *Cadence Design Systems, Inc.*

This year, the traditional ICCAD panel explores a topic dear to the hearts of ICCAD attendees: the publication process. Are hardcopy, paper publications still relevant? Are journals themselves still relevant, or is the distinction between conference and journal publication an anachronism?

How do the economics of publishing influence journal “page quotas”, publication access, and the editorial process itself? Are changes to traditional publication models viable in the context of the academic tenure and promotion process? What is the future of electronic publication and archiving? The panel will explore these, and other, questions related to publication in engineering.

Come prepared for a lively discussion on the future of publication in the electronic design automation community.

Panelists: Barbara Lange - *IEEE*
Sachin Sapatnekar - *Univ. of Minnesota*
John Willinsky - *Stanford Univ.*

Monday, November 2, 2009

ACM/SIGDA Member Meeting

7:30pm - Siskiyou Ballroom

INVITED SPEAKER: Martin Davis, New York Univ.

2009 SIGDA Pioneering Achievement Award Recipient

Please join us for a unique event with Martin Davis, the recipient of this year's SIGDA Pioneering Achievement Award for his outstanding contributions to algorithms for solving the Boolean Satisfiability problem, which heavily influenced modern tools for hardware and software verification, as well as logic synthesis.

Please join us!



Meetings at ICCAD

Sunday, November 1

The ACM/SIGDA CADathlon

7:30am – 5:00pm
Donner Ballroom

Monday, November 2

The Future of EDA--A conversation with Jim Hogan and Paul McLellan on what EDA needs to change to succeed

3:00 - 4:00pm
Silicon Valley Room

ACM/SIGDA Member Meeting

7:30 - 9:30pm
Siskiyou Ballroom

47th DAC Technical Program Committee Meeting

7:30 - 10:00pm
Donner Ballroom

Tuesday, November 3

47th DAC Exhibitor Meeting

1:00 - 2:00pm
San Jose/Santa Clara Room

Time: 8:30 AM - 10:00 AM

Room: Oak

SESSION 4A • TUTORIAL: INTRODUCTION TO GPU PROGRAMMING FOR EDA

Advances in GPU technology have propelled the GPU into arenas far afield from the traditional, isolated roles they have previously played. With dozens to hundreds of processing units in a single GPU, substantial speedups can be achieved by harnessing their power to augment the performance of the traditional single- or multi-core CPU. However, utilizing the GPU requires both a change in the programmer's traditional algorithmic model as well as a judicious selection of problem type. This tutorial reviews the GPU architecture and the tools available to utilize this valuable resource. It also provides insight into the type of problem best suited for the GPU as well as programming styles required to fully harness the power of the GPU. We present examples of specific EDA algorithms that can benefit from GPU acceleration, using both the CUDA and OpenCL environments.

Presenters: **John F. Croix** - *Cadence Design Systems, Inc.*
Sunil P. Khatri - *Texas A&M Univ.*

Time: 8:30 AM - 10:00 AM

Room: Fir

SESSION 4B • ANALYTICAL ADVANCES IN PHYSICAL SYNTHESIS

Moderators: **Masanori Hashimoto** - *Osaka Univ.*
Yao-Wen Chang - *National Taiwan Univ.*

This session discusses various analytical advances in physical synthesis and optimization. The first paper proposes a provably near-optimal algorithm for discrete Vt assignment for leakage power minimization. It is followed by a paper that presents a class of timing-driven net weighting schemes and a set of criteria that guarantees such net weights to converge to a local optimum. The third paper in the session proposes a fast NlogN technique for full-chip leakage analysis considering spatial correlations of process parameters.

4B.1 B THE EPSILON-APPROXIMATION TO DISCRETE VT ASSIGNMENT FOR LEAKAGE POWER MINIMIZATION

Yujia Feng, **Shiyan Hu** (shiyan@mtu.edu) - *Michigan Technological Univ.*

4B.2 A RIGOROUS FRAMEWORK FOR CONVERGENT NET WEIGHTING SCHEMES IN TIMING-DRIVEN PLACEMENT

Tony F. Chan, Jason Cong, **Eric Radke** (radke@math.ucla.edu) - *Univ. of California, Los Angeles*

4B.3 AN EFFICIENT ALGORITHM FOR MODELING SPATIALLY-CORRELATED PROCESS VARIATION IN STATISTICAL FULL-CHIP LEAKAGE ANALYSIS

Zuochang Ye (zuochang@tsinghua.edu.cn), Zhiping Yu - *Tsinghua Univ.*

Time: 8:30 AM - 10:00 AM

Room: Pine

SESSION 4C • THERMAL-AWARE MANAGEMENT TECHNIQUES FOR MULTI-CORE ARCHITECTURES

Moderators: Ayse K. Coskun - *Boston Univ.*
Jose L. Ayala - *Univ. Complutense Madrid*

This session focuses on thermal-aware management techniques for multi-core architectures. The first paper proposes an agent-based power distribution approach that aims to balance the power consumption and thermal distribution in a pro-active way. The second paper of the session extends the formulation of the problem of minimizing the completion time of tasks in multi-core processors with thermal constraints and leakage dependence on temperature. The last paper proposes a hybrid local-global thermal management approach that employs DVFS across all the cores, but locally tunes the performance/temperature tradeoff of each core individually through architectural adaptations.

4C.1 B TAPE: THERMAL-AWARE AGENT-BASED POWER ECONOMY FOR MULTI/MANY-CORE ARCHITECTURES

Thomas Ebi (ebi@informatik.uni-karlsruhe.de), Mohammad Abdullah Al Faruque, Jörg Henkel - *Univ. Karlsruhe*

4C.2 MAXIMIZING PERFORMANCE OF THERMALLY CONSTRAINED MULTI-CORE PROCESSORS BY DYNAMIC VOLTAGE AND FREQUENCY CONTROL

Vinay Hanumaiah (vinayh@asu.edu), Sarma Vrudhula, Karam Chatha - *Arizona State Univ.*

4C.3 A HYBRID LOCAL-GLOBAL APPROACH FOR MULTI-CORE THERMAL MANAGEMENT

Ramkumar Jayaseelan (ramkumar@comp.nus.edu.sg), Tulika Mitra - *National Univ. of Singapore*

Time: 8:30 AM - 10:00 AM

Room: Cedar

DESIGNER TRACK • WHEN SPICE IS NOT ENOUGH

This session discusses the problems faced by analog designers when the circuits they build must interact with complex non-analog or non-electronic systems. These other portions of the systems can span a wide range, from digital signal processing, to software, to mechanical or biological systems. This session covers the travails of three designers, each building analog circuits in one or more of these domains. Each will describe the specific problems they face, how they approach these problems with existing tools, and what they would like for the tools of the future.

Global Convergence Failures in "Digi-Log" Circuits

Presenter: **Jaeha Kim** - *Stanford Univ.*

Today's analog circuits are in fact mixed-signal circuits, employing digital circuits to some extent to tune out the non-idealities. Designers of such digitally-assisted analog (or "digi-log") circuits, however, have encountered various start-up failures due to the nonlinear nature of the digital components. For example, a digital PLL or CDR may experience various lock failures depending on how it is turned on. While the similar start-up failures in purely digital systems are effectively prevented by using the notion of indeterminate states (known as 'X') during simulation, no similar concepts exist for SPICE-like analog simulators. This talk examines common start-up failures in PLLs. By recognizing them as global convergence failures, it then discusses possible approaches to detect them during design time, possibly saving millions in respinning the chips.

Designing in a Multi-Physics Environment

Presenter: **Bill Clark** - *Analog Devices, Inc.*

Designing products increases in difficulty when crossing physical domains. Modeling, simulation, and analysis tools that address the entire problem space are either absent or ineffective. Even the engineers working different facets of the problem hardly speak the same language. Finding the common ground and coordinating work across disciplines is the essential to a successful product development.

All speakers are denoted in bold
S - denotes short paper
B - denotes best paper candidate

Tuesday, November 3, 2009

Time: 8:30 AM - 10:00 AM

Room: Cedar

DESIGNER TRACK • WHEN SPICE IS NOT ENOUGH (CONT.)

Bioelectronic Systems Design

Presenter: **Kenneth Shepard** - *Columbia Univ.*

Integrated circuits based on CMOS technology have been the engine for the computation and communication of the last 40 years. As technology scaling comes to an end, the future of integrated circuit design lies in finding new applications, primarily in the life sciences, that have been largely ignored in the quest for faster and denser processing and communications devices. In this talk, I will describe emerging IC applications involving direct interfaces with biological and biomolecular systems. Examples include solid-state nanopores, electrowetting-based microfluidics, active sensing arrays for DNA and protein assays, and novel imagers and actuators that interface directly with cells and tissue. These systems present unique simulation and modelling challenges, leading to a convergence of CAD tools from different disciplines, SolidWorks, COMSOL, Matlab along with traditional EDA software. Unique CAD opportunities will be created by this growing convergence and the importance of multi-domain design.

Presenters: **Jaeha Kim** - *Stanford Univ.*
Bill Clark - *Analog Devices, Inc.*
Kenneth Shepard - *Columbia Univ.*

Time: 8:30 AM - 10:00 AM

Room: Donner

SESSION 4E • TUTORIAL: ANALYSIS AND TESTING OF CONCURRENT PROGRAMS

Hardware advances have forced programmers to develop concurrent software. Unfortunately, concurrent programs are extremely hard to write, analyze, test, and debug. CHES is a research platform developed at Microsoft Research to address many of these challenges. CHES works on user-mode native (C/C++) or managed (C#) programs and has demonstrably scaled to large industrial-scale software. CHES can predictably and systematically drive a given program along a specified set of thread interleavings. This predictable control allows CHES to successfully find and reproduce concurrency errors. These "Heisenbugs" are otherwise very hard to find or reproduce.

Over the past three years, CHES has matured as an extensible platform for building analysis tools for concurrency. This tutorial will provide hands-on experience in using the various features of this platform. The tutorial will also demonstrate ways to build custom analysis tools and interleaving search strategies using CHES. Researchers interested in concurrency analysis and testing, and educators interested in teaching concurrency should find this tutorial helpful. CHES is available for download with an academic license at <http://research.microsoft.com/CHES>.

In this tutorial, the audience will learn the following:

1. How to use CHES to systematically test concurrent programs
2. How to reproduce concurrency errors/Heisenbugs that are otherwise hard to reproduce
3. How to use CHES for dynamic analysis of concurrent programs, such as detecting data races, atomicity violations, and memory consistency errors
4. How to extend CHES with various search-heuristics for finding errors in concurrent programs

Presenters: **Madan Musuvathi, Shaz Qadeer** - *Microsoft Corp.*

Time: 10:30 AM - 12:00 PM

Room: Oak

SESSION 5A • STATISTICAL TIMING ANALYSIS AND ITS APPLICATION

Moderators: Xin Li - *Carnegie Mellon Univ.*
Yaping Zhan - *Advanced Micro Devices, Inc.*

This session discusses new algorithms and methodologies for statistical timing analysis and its applications. The first paper proposes an efficient algorithm to handle topological correlation for statistical timing analysis. The second paper develops an optimal scheme to determine speed bins based on timing analysis results. The final paper extracts accurate-yet-simple timing models to enable hierarchical timing analysis with consideration of large-scale process variations.

5A.1 B A HIERARCHY OF SUBGRAPHS UNDERLYING A TIMING GRAPH AND ITS USE IN CAPTURING TOPOLOGICAL CORRELATION IN SSTA

Jaeyong Chung (jwings@gmail.com), Jacob A. Abraham - *Univ. of Texas, Austin*

5A.2 BINNING OPTIMIZATION BASED ON SSTA FOR TRANSPARENTLY-LATCHED CIRCUITS

Min Gong (gongmin@fudan.edu.cn) - *Fudan Univ.*
Hai Zhou - *Northwestern Univ.*
Jun Tao, Xuan Zeng - *Fudan Univ.*

5A.3 TIMING MODEL EXTRACTION FOR SEQUENTIAL CIRCUITS CONSIDERING PROCESS VARIATIONS

Bing Li (b.li@tum.de), Ning Chen, Ulf Schlichtmann - *Technische Univ. München*

Time: 10:30 AM - 12:00 PM

Room: Fir

SESSION 5B • CONGESTION DRIVEN PLACEMENT

Moderators: Saurabh Adya - *Synopsys, Inc.*
Matt Guthaus - *Univ. of California, Santa Cruz*

Congestion is a major concern in modern placement; wire length alone is not a sufficient metric. The papers in this session explore ways to alter placement to improve routing. The first three papers use a variety of techniques to model routing congestion and spread placements, while the last performs a study of the relative importance of these techniques.

5B.1 B CROP: FAST AND EFFECTIVE CONGESTION REFINEMENT OF PLACEMENT

Yanheng Zhang (zyh@iastate.edu), Chris Chu - *Iowa State Univ.*

5B.2 GRPLACER: IMPROVING ROUTABILITY AND WIRE-LENGTH OF GLOBAL ROUTING WITH CIRCUIT REPLACEMENT

Ke-Ren Dai (dkr.cs96g@nctu.edu.tw) - *National Chiao-Tung Univ.*
Chien-Hung Lu - *SpringSoft, Inc.*
Yih-Lang Li - *National Chiao-Tung Univ.*

5B.3S CRISP: CONGESTION REDUCTION BY ITERATED SPREADING DURING PLACEMENT

Jarrold A. Roy (royj@eecs.umich.edu) - *Univ. of Michigan*
Natarajan Viswanathan, Gi-Joon Nam, Charles J. Alpert - *IBM Corp.*
Igor L. Markov - *Univ. of Michigan*

5B.4S A STUDY OF ROUTABILITY ESTIMATION AND CLUSTERING IN PLACEMENT

Kalliopi Tsota (ktsota@purdue.edu), Cheng-Kok Koh, Venkataramanan Balakrishnan - *Purdue Univ.*

Time: 10:30 AM - 12:00 PM

Room: Pine

SESSION 5C • NEW APPLICATIONS IN LOGIC SYNTHESIS

Moderators: Rolf Drechsler - *Univ. of Bremen*
Sunil P. Khatri - *Texas A&M Univ.*

This session presents three papers which outline applications of Logic Synthesis approaches. The first paper uses logic approaches to synthesize probabilities. The second presents an approach to perform retiming in the context of pulsed-latch based designs. The last paper presents approaches to synthesize a complementary dual of a given circuit.

5C.1 THE SYNTHESIS OF COMBINATIONAL LOGIC TO GENERATE PROBABILITIES

Weikang Qian (qianx030@umn.edu), Marc D. Riedel, Kia Bazargan, David J. Lilja - *Univ. of Minnesota*

5C.2 RETIMING AND TIME BORROWING: OPTIMIZING HIGH-PERFORMANCE "PULSED-LATCH BASED" CIRCUITS

Seonggwon Lee, **Seungwhun Paik** (swpaik@dtlab.kaist.ac.kr), Youngsoo Shin - *KAIST*

5C.3 SYNTHESIZING COMPLEMENTARY CIRCUITS AUTOMATICALLY

ShengYu Shen (shengyushen@gmail.com), JianMin Zhang, Ying Qin, SiKun Li - *National Univ. of Defense Technology*

Time: 10:30 AM - 12:00 PM

Room: Cedar

DESIGNER TRACK • PRACTICAL EXPERIENCE AND FUTURE TOOL DIRECTIONS AT NEW PROCESS NODES

This session discusses the practical problems faced by designers trying to build state-of-the-art products using the existing tools. As always, each new process generation brings new problems that the tools are not quite ready to address, and designers must work around these issues with some combination of methodology, custom tools, clever techniques, and plain old elbow grease. The experience of these designers is exceedingly valuable to those who strive to build new tools, since these designers have already been forced to confront the design issues of new process nodes under the constraints of tight time to market.

Challenges of designing robust IP at 22nm

Presenter: **Vikas Chandra** - *ARM Ltd.*

As we move into the 22nm era, the design of robust IP becomes increasingly challenging. Without substantial improvement in lithography capabilities, 22nm design becomes heavily constrained by fundamental printing issues and increased variability. Other historical trends such as those in reliability and BEOL scaling also continue to become increasingly problematic. These difficulties are typically addressed via margining and restrictive design rules; however those methods are often not amenable to designing IP with optimal size, speed and power. In this talk, I will discuss these challenges and our approach to creating robust and high-performance physical IP at 22nm.

Beyond Design...Challenges of IA Platform Productization

Presenter: **Keshavan "K7" Tiruvallur** - *Intel Corp.*

Post-Si validation challenges loom large as platforms see increased levels of integration resulting in significantly less visibility outside the silicon. Gone are the days when a single Front Side Bus Logic Analyzer trace was enough to root cause and solve any platform related failures. In addition to integration IO speeds and tricky circuits make it harder to optimally margin (electrically) platforms. A large portion of the silicon must work off the bat in order to sustain a predictable product launch schedule which continues to compress in time. This talk exposes some of the challenges with a plea for help from the CAD community.

Time: 12:00 PM

Siskiyou Ballroom

Smart Grid for the 21st Century

Organizer: Shishpal Rawat - Intel Corp.

Presenter: Byron Washom - Univ. of California, San Diego

The Obama Administration is currently evaluating proposals submitted in response to a \$4.5B program to launch the next generation of how electricity is produced, transmitted, distributed, stored and used in a more secure, efficient and intelligent manner. The "Smart Grid" functions and qualifying investments sought by DOE centered on measuring, metering, monitoring, communicating and analyzing data at unprecedented levels while maintaining cyber security. The precursors to the future full scale Smart Grid visions are "microgrids" operated by large industrial customers of utilities like UC San Diego that only imports 20% of its total electricity demand. The presentation will discuss UC San Diego's pioneering projects to meet 20% of its supply from renewable energy, accomplish 20% permanent load shifting through energy storage, and reduce its demand through C3 technologies.

Mr. Byron Washom is UC San Diego's Director of Strategic Energy Initiatives and previously served as Sr. International Advisors to DOE and the World Bank as well as a due diligence examiner of clean technologies to a global clientele of utilities, investors, and institutions for over twenty years. In 1984, Mr. Washom received an IR100 Award for having set the world's record for solar energy conversion that remained unsurpassed for 24 years. Mr. Washom is a four time Rockefeller Foundation grantee and a Heinz Endowment grantee.

Sponsored By:



Time: 1:30 PM - 3:30 PM

Room: Oak

SESSION 6A • ADVANCED MODELING AND SIMULATION METHODS

Moderators: Frank Liu - IBM Corp.
Eric J. Grimme - Intel Corp.

This session showcases recent developments on modeling and simulation of electrical and biochemical circuits and systems. The first paper proposes advanced nonlinear model order reduction techniques. The second paper presents advanced theory and numerical methods for oscillator analysis. Finally, parallel circuit simulation is facilitated by solving final-value ODEs and parallel preconditioning techniques in the third and fourth presentations.

- 6A.1 QLMOR: A NEW PROJECTION-BASED APPROACH FOR NONLINEAR MODEL ORDER REDUCTION**
Chenjie Gu (gcj@eecs.berkeley.edu) - Univ. of California, Berkeley
- 6A.2 COMPUTING QUADRATIC APPROXIMATIONS FOR THE ISOCHRONS OF OSCILLATORS: A GENERAL THEORY AND ADVANCED NUMERICAL METHODS**
Onder Suvak (osuvak@ku.edu.tr), Alper Demir - Koc Univ.
- 6A.3 FINAL-VALUE ODES: STABLE NUMERICAL INTEGRATION AND ITS APPLICATION TO PARALLEL CIRCUIT ANALYSIS**
Wei Dong, **Peng Li** (pli@neo.tamu.edu) - Texas A&M Univ.
- 6A.4 A PARALLEL PRECONDITIONING STRATEGY FOR EFFICIENT TRANSISTOR-LEVEL CIRCUIT SIMULATION**
Heidi K. Thornquist (hkthorn@sandia.gov), Eric R. Keiter, Robert J. Hoekstra, David M. Day, Erik G. Boman - Sandia National Labs

Time: 1:30 PM - 3:30 PM

Room: Fir

SESSION 6B • CHARACTERIZATION AND COMPENSATION OF VARIABILITY

Moderator: Azadeh Davoodi - *Univ. of Wisconsin*

This session presents latest work on variability characterization and compensation. The first paper proposes a new measurement technique for identifying the intra-chip spatial variation profile. The second paper presents an application of condensed sensing to effective measurement of process variability. The final paper describes an estimation and optimization methods for voltage binning.

6B.1 CHARACTERIZING WITHIN-DIE VARIATION FROM MULTIPLE SUPPLY PORT IDDQ MEASUREMENTS

Kanak Agarwal - *IBM Corp.*

Dhruva Acharyya (djacharyya@gmail.com) - *Verigy, Inc.*

Jim Plusquellic - *Univ. of New Mexico*

6B.2 VOLTAGE BINNING UNDER PROCESS VARIATION

Vladimir Zolotov (zolotov@us.ibm.com), Chandu Visweswariah, Jinjun Xiong - *IBM Corp.*

6B.3 VIRTUAL PROBE: A STATISTICALLY OPTIMAL FRAMEWORK FOR MINIMUM-COST SILICON CHARACTERIZATION OF NANOSCALE INTEGRATED CIRCUITS

Xin Li (xinli@ece.cmu.edu), Rob Rutenbar, Shawn Blanton - *Carnegie Mellon Univ.*

6B.4 POST-FABRICATION MEASUREMENT-DRIVEN OXIDE BREAKDOWN RELIABILITY PREDICTION AND MANAGEMENT

Cheng Zhuo (hzzc1012@hotmail.com), David Blaauw, Dennis Sylvester - *Univ. of Michigan*

Time: 1:30 PM - 3:30 PM

Room: Pine

SESSION 6C • POLICIES AND METHODS FOR LOW POWER

Moderator: Li Shang - *Univ. of Colorado, Boulder*

This session explores policies and techniques to develop energy efficient circuits and systems. It is increasingly necessary to consider alternate methods and policies that reduce power and energy consumption. Some of the policies and methods that will be discussed in this session include integration of DVS and DPM, adaptive power management, wakeup scheduling and circuit clustering for leakage control.

6C.1 MINIMIZING EXPECTED ENERGY CONSUMPTION THROUGH OPTIMAL INTEGRATION OF DVS AND DPM

Baoxian Zhao (bzhao@gmu.edu), Hakan Aydin - *George Mason Univ.*

6C.2 AN EFFICIENT WAKEUP SCHEDULING CONSIDERING RESOURCE CONSTRAINT FOR SENSOR-BASED POWER GATING DESIGNS

Ming-Chao Lee (mingchao.lee@gmail.com), Yu-Ting Chen, Yo-Tzu Cheng, Shih-Chieh Chang - *National Tsing-Hua Univ.*

6C.3 ADAPTIVE POWER MANAGEMENT USING REINFORCEMENT LEARNING

Ying Tan, Wei Liu, **Qinru Qiu** (qinru.qiu@gmail.com) - *Binghamton Univ.*

6C.4 TEMPORAL AND SPATIAL IDLENESS EXPLOITATION FOR OPTIMAL-GRAINED LEAKAGE CONTROL

Hao Xu (xuhu@email.uc.edu), Ranga Vemuri, Wen-Ben Jone - *Univ. of Cincinnati*

Time: 1:30 PM - 3:30 PM

Room: Cedar

SESSION 6D • EMERGING MEMORY TECHNOLOGIES

Moderators: Elad Alon - *Univ. of California, Berkeley*
Dejan Markovic - *Univ. of California, Los Angeles*

This session presents novel ideas in memory design. The first paper presents design tradeoffs in non-volatile spin-torque transfer based memories. The second paper proposes the use of nano-mechanical relays for low-leakage SRAMs. The third paper explores the use of memristor technology for future non-volatile memories. The fourth paper presents simulation environment for genetic memory networks.

6D.1 A METHODOLOGY FOR ROBUST, ENERGY EFFICIENT DESIGN OF SPIN-TORQUE-TRANSFER RAM ARRAYS AT SCALED TECHNOLOGIES

Subho Chatterjee (subho.chatterjee@gatech.edu), Michelle Rasquinha, Sudhakar Yalamanchili, Saibal Mukhopadhyay - *Georgia Institute of Technology*

6D.2 NANO-ELECTROMECHANICAL (NEM) RELAY INTEGRATED WITH CMOS SRAM FOR IMPROVED STABILITY AND LOW LEAKAGE

Soogine Chong (sgchong@stanford.edu), Kerem Akarvardar, Roozbeh Parsa - *Stanford Univ.*
Jun-Bo Yoon - *KAIST*
Subhasish Mitra, Roger T. Howe, H.-S. Philip Wong - *Stanford Univ.*

6D.3 NONVOLATILE MEMRISTOR MEMORY: DEVICE CHARACTERISTICS AND DESIGN IMPLICATIONS

Yenpo Ho (ypho@neo.tamu.edu), Garni Huang, Peng Li - *Texas A&M Univ.*

6D.4 GENE-REGULATORY MEMORIES: ELECTRICAL-EQUIVALENT MODELING, SIMULATION AND PARAMETER IDENTIFICATION

Yong Zhang (zhangyong@neo.tamu.edu), Peng Li - *Texas A&M Univ.*

Time: 1:30 PM - 3:30 PM

Room: Donner

SESSION 6E • SPECIAL SESSION: POWER 7 - VERIFICATION CHALLENGES OF A HIGH-END 8-CORE MICROPROCESSOR

Over the years functional hardware verification has made significant progress in the areas of traditional simulation techniques, accelerator usage and last but not least formal verification approaches. This has been sufficient to deal with the additional content and complexity increase that has been happening at the same time.

For Power 7, IBM's first high end 8-core microprocessor, the incremental improvements have been deemed not to be enough by themselves, because the chip was not just a remap of an existing design with more cores. The infrastructure on the chip had to be changed significantly, while at the same time the business side requested a shorter development cycle with perfect quality but without growing the team. Looking at these constraints a two phase approach seemed to be the only solution.

This tutorial commences with the highlights of the first phase, where improvements to the existing process have been identified. This includes topics ranging from enhanced test case generation, over advancements in structural checking and the conversion of architectural checks for acceleration, to the extensions of the formal verification scope both in property checking and sequential equivalence checking.

Subsequently, the tutorial is describing the second phase which has been geared towards synergy exploitation across the various verification activities. The interlocks between simulation, formal verification and acceleration have led to new innovations that improved the overall verification process and helped with the resource constraints.

Finally, the results of this approach as observed in the Power 7 project are discussed and an outlook regarding future trends is given.

6E.1 POWER 7 - VERIFICATION CHALLENGE OF A MULTI-CORE PROCESSOR

Klaus-Dieter Schubert - *IBM Deutschland Research and Development GmbH*

Time: 4:00 PM - 6:00 PM

Room: Oak

SESSION 7A • ADVANCED DEVICE RELIABILITY AND MODELING

Moderators: Bruce W. McGaughy - *Proplus Design Solutions, Inc.*
Eric R. Keiter - *Sandia National Labs*

This session focuses on advanced device reliability and modeling techniques. The first paper proposes a novel repair methodology considering end-of-life yield improvement. The second paper presents techniques for modeling Finfet-based devices and variability. Finally, the third and fourth papers discuss the modeling layout-dependent stress effects and its application in circuit optimization.

7A.1 B AN ELEGANT HARDWARE-CORROBORATED STATISTICAL REPAIR AND TEST METHODOLOGY FOR CONQUERING AGING EFFECTS

Rouwaida Kanj (rouwaida@us.ibm.com), Rajiv Joshi, Chad Adams, James Warnock, Sani Nassif - *IBM Corp.*

7A.2 VARIABILITY ANALYSIS OF FINFET-BASED DEVICES AND CIRCUITS CONSIDERING ELECTRICAL CONFINEMENT AND WIDTH QUANTIZATION

Seid Hadi Rasouli (hadi@ece.ucsb.edu) - *Univ. of California, Santa Barbara*
Kazuhiko Endo - *Advanced Industrial Science and Technology*
Kaustav Banerjee - *Univ. of California, Santa Barbara*

7A.3S MODELING OF LAYOUT-DEPENDENT STRESS EFFECT IN CMOS DESIGN

Chi-Chao Wang (cwwang73@asu.edu), Wei Zhao - *Arizona State Univ.*
Frank Liu - *IBM Corp.*
Min Chen, Yu Cao - *Arizona State Univ.*

7A.4S LAYOUT-DEPENDENT STI STRESS ANALYSIS AND STRESS-AWARE RF/ANALOG CIRCUIT DESIGN OPTIMIZATION

Jiying Xue (xuejy06@mails.tsinghua.edu.cn), Zuochang Ye, Yangdong Deng, Liu Yang, Hongrui Wang, Zhiping Yu - *Tsinghua Univ.*

Time: 4:00 PM - 6:00 PM

Room: Fir

SESSION 7B • CLOCK OPTIMIZATION AND PARALLEL ALGORITHM IN EDA

Moderators: Lars Hagen - *Cadence Design Systems, Inc.*
Shiyan Hu - *Michigan Technical Univ.*

This session discusses advances in clock skew minimization and parallel GPU computing for EDA. The first paper introduces a new optimization paradigm of asynchronous parallel pattern search (APPS) method to CAD, and uses it to solve the clock mesh skew minimization problem. A new technique for skew minimization is performed by using adjustable delay buffers in the second paper, which has an added advantage of being applicable to the problem in the multi-voltage domain. The third paper provides a parallel technique for sparse-matrix vector product that is implementable on GPUs, and can be applied to EDA problems. In the fourth paper, multilevel clustering is used for skew optimization in a discrete set of domains.

7B.1 LEVERAGING EFFICIENT PARALLEL PATTERN SEARCH FOR CLOCK MESH OPTIMIZATION

Xiaoji Ye (yexiaoji@neo.tamu.edu), Srinath Narasimhan, Peng Li - *Texas A&M Univ.*

7B.2 VALUE ASSIGNMENT OF ADJUSTABLE DELAY BUFFERS FOR CLOCK SKEW MINIMIZATION IN MULTI-VOLTAGE MODE DESIGNS

Yu-Shih Su, Wing-Kai Hon, Cheng-Chih Yang, Shih-Chieh Chang - *National Tsing-Hua Univ.*
Yeong-Jar Chang - *Faraday Technology Corp.*
Yu-Chien Kao (yckao@nthu.us) - *National Tsing-Hua Univ.*

7B.3 TAMING IRREGULAR EDA APPLICATIONS ON GPUS

Yangdong Deng (dengyd@tsinghua.edu.cn), Bo Wang, Shuai Mu - *Tsinghua Univ.*

7B.4 MULTI-LEVEL CLUSTERING FOR CLOCK SKEW OPTIMIZATION

Jonas Casanova (jcasanova@lsi.upc.edu), Jordi Cortadella - *Univ. Politecnica de Catalunya*

Time: 4:00 PM - 6:00 PM

Room: Pine

SESSION 7C • ANALYSIS AND OPTIMIZATION OF NETWORK-ON-CHIP AND MULTIPROCESSOR SOC

Moderator: Umit Y. Ogras - *Intel Corp.*

The session presents recent research results concerning the analysis and design optimization of modern multiprocessor and NOC architectures. Four of the papers deal with Network on Chip systems. The first presentation compares 2-D and 3-D integration technologies for mesh-based NOCs. Using both analytical methods and simulation, the Authors analyze the impact of 2-D and 3-D technology on the worst-case performance of the network. The second and third paper derive queuing models for NOC systems. The main concern of the second paper is high accuracy as well as the consideration of virtual channels. The third paper presents new analytical models in the context of constant service time routers. The fourth paper considers the issue of guaranteed QOS for systems implemented on NOC architectures. The final presentation introduces an application-specific processor aimed at accelerating the scheduling, mapping, and synchronization of tasks in a multiprocessor system-on-chip.

7C.1 B FROM 2-D TO 3-D NOCS: A CASE STUDY ON WORST-CASE COMMUNICATION PERFORMANCE

Yue Qian (qy.nudt@gmail.com) - *National Univ. of Defense Technology*
Zhonghai Lu - *Royal Institute of Technology*
Wenhua Dou - *National Univ. of Defense Technology*

7C.2 AN ACCURATE AND EFFICIENT PERFORMANCE ANALYSIS APPROACH BASED ON QUEUING MODEL FOR NETWORK-ON-CHIP

Mingche Lai (mingchelai@nudt.edu.cn), Lei Gao, Nong Xiao, Zhiying Wang - *National Univ. of Defense Technology*

7C.3 A PERFORMANCE ANALYTICAL MODEL FOR NETWORK-ON-CHIP WITH CONSTANT SERVICE TIME ROUTERS

Nikita Nikitin (nnikitin@lsi.upc.edu), Jordi Cortadella - *Univ. Politecnica de Catalunya*

7C.4S A METHOD FOR CALCULATING HARD QOS GUARANTEES FOR NETWORKS-ON-CHIP

Dara Rahmati - *Sharif Univ. of Technology*
Srinivasan Murali - *iNOC, LSI and Ecole Polytechnique Federale de Lausanne*
Luca Benini - *Univ. di Bologna*
Federico Angiolini (angiolini@inocs.com) - *iNOCs*
Giovanni De Micheli - *Ecole Polytechnique Federale de Lausanne*
Hamid Sarbazi-azad - *Institute for Research in Fundamental Sciences*

7C.5S TASK MANAGEMENT IN MPSoCs: AN ASIP APPROACH

Jerónimo Castrillon (jeronimo.castrillon@iss.rwth-aachen.de), Diandian Zhang, Torsten Kempf - *RWTH Aachen Univ.*
Bart Vanthournout - *CoWare, Inc.*
Rainer Leupers, Gerd Ascheid - *RWTH Aachen Univ.*

Time: 4:00 PM - 6:00 PM

Room: Cedar

SESSION 7D • DESIGN-PATTERNING INTERACTIONS

Moderators: Nagib Hakim - *Intel Corp.*
Michael Orshansky - *Univ. of Texas, Austin*

This session presents four papers to deal with interactions between lithographic patterning and design. The first three papers talk about double patterning lithography (DPL). The first paper proposes a method to simultaneously address the problems of layout migration and layout decomposition for double patterning. The second paper proposes an interesting graph reduction technique to speed up DPL decomposition. The third paper addresses DPL coloring problem in conjunction with its timing impact. The session concludes with a paper discussing systematic co-exploration of design rules, technology and layout choices.

7D.1 SIMULTANEOUS LAYOUT MIGRATION AND DECOMPOSITION FOR DOUBLE PATTERNING TECHNOLOGY

Chin-Hsiung Hsu (ariou@s@eda.ee.ntu.edu.tw), Yao-Wen Chang - *National Taiwan Univ.*
Sani Nassif - *IBM Corp.*

7D.2 GREMA: GRAPH REDUCTION BASED EFFICIENT MASK ASSIGNMENT FOR DOUBLE PATTERNING TECHNOLOGY

Yue Xu (yuexu@iastate.edu), Chris Chu - *Iowa State Univ.*

7D.3 TIMING YIELD-AWARE COLOR REASSIGNMENT AND DETAILED PLACEMENT PERTURBATION FOR DOUBLE PATTERNING LITHOGRAPHY

Mohit Gupta, **Kwangok Jeong** (kjeong@vlsicad.ucsd.edu), Andrew B. Kahng - *Univ. of California, San Diego*

7D.4 A FRAMEWORK FOR EARLY AND SYSTEMATIC EVALUATION OF DESIGN RULES

Rani S. Ghaida (rani@ee.ucla.edu), Puneet Gupta - *Univ. of California, Los Angeles*

Time: 4:00 PM - 6:00 PM

Room: Donner

SESSION 7E • SPECIAL SESSION: STATISTICAL TIMING: WHERE IS THE TOFU?

For over 5 years, there have been numerous papers on the topic of Statistical Static Timing Analysis (SSTA), and several product offerings. But does it really work in practice? What are the benefits of statistical sign-off? What are the pitfalls? How does one optimize towards statistical sign-off? As we transition to 32 nm, is multi-corner timing running out of steam? Are we marginalizing our business by margining? Our industry is at a crucial juncture at which these questions must be answered.

This special session will use real timing data from several industrial 65 nm ASICs to answer these questions. Collective experience from statistical sign-off across two generations of technology will be shared. Details of the SSTA tool and methodology used in the study will be presented. Real timing data will be used to compare and contrast four timing methodologies: two-corner timing, multi-corner timing, exhaustive corner timing and SSTA. The value-add, pessimism incurred and concomitant margining in each of these flows will be spelled out with supporting data.

The special session will consist of four presentations. The first talk will describe the SSTA tool and how it was validated against multi-corner timing. The second presentation will discuss performance improvements and introduce the concept of statistical projection. The third talk will lay out a sign-off flow with a reduced number of timing runs required for sign-off with numerous pessimism reduction techniques and describe how the flow is crafted for ease of use. The value-add of statistical timing will be studied in the final presentation by comparing it to two-corner, multi-corner and exhaustive corner timing flows.

7E.1 STATISTICAL TIMING FOR FULL-PROCESS COVERAGE: A TOOL PERSPECTIVE

Jinjun Xiong - IBM T.J. Watson Research Center

7E.2 MAKING STATISTICAL TIMING PRACTICAL

Vladimir A. Zolotov - IBM T.J. Watson Research Center

7E.3 VARIATION-DRIVEN TIMING METHODOLOGY WITH REDUCED PESSIMISM

Eric A. Foreman - IBM T.J. Watson Research Center

7E.4 HERE COMES THE TOFU: THE VALUE OF STATISTICAL TIMING

Chandu Visweswariah - IBM T.J. Watson Research Center

All speakers are denoted in bold
S - denotes short paper
B - denotes best paper candidate

Wednesday, November 4, 2009

Time: 8:30 AM - 10:00 AM

Room: Oak

SESSION 8A • YIELD ESTIMATION AND OPTIMIZATION FOR SRAMS

Moderators: Eric R. Keiter - *Sandia National Labs*
Saurabh K. Tiwary - *Cadence Design Systems, Inc.*

This session presents advances in SRAM yield analysis and optimization. The first paper proposes speeding up techniques for importance-sampling based yield analysis. The second paper presents a "Virtual Fab" integration framework for yield estimation and finally the last paper proposes optimization methodologies for adaptive voltage architecture.

8A.1 ADAPTIVE SAMPLING FOR EFFICIENT FAILURE PROBABILITY ANALYSIS OF SRAM CELLS

Javid Jaffari (jjaffari@vlsi.uwaterloo.ca), Mohab Anis - *Univ. of Waterloo*

8A.2 YIELD ESTIMATION OF SRAM CIRCUITS USING "VIRTUAL SRAM FAB"

Aditya Bansal (bansal@us.ibm.com), Rama N. Singh - *IBM T.J. Watson Research Center*

Rouwaida N. Kanj - *IBM Corp.*

Saibal Mukhopadhyaya - *Georgia Institute of Technology*

Jin-Fuw Lee - *IBM T.J. Watson Research Center*

Emrah Acar, Amith Singhe - *IBM Corp.*

Keunwoo Kim - *IBM T.J. Watson Research Center*

Ching-Te Chuang - *National Chiao-Tung Univ.*

Koushik Das, Fook-Luen Heng - *IBM T.J. Watson Research Center*

Sani Nassif - *IBM Corp.*

8A.3 MITIGATION OF INTRA-ARRAY SRAM VARIABILITY USING ADAPTIVE VOLTAGE ARCHITECTURE

Ashish K. Singh (aksingh@cerc.utexas.edu), Ku He, Constantine Caramanis, Michael Orshansky - *Univ. of Texas, Austin*

Time: 8:30 AM - 10:00 AM

Room: Fir

SESSION 8B • THERMAL MODELING AND ANALYSIS AT CHIP AND PLATFORM LEVELS

Moderator: Arijit Raychowdhury - *Intel Corp.*

This session covers thermal modeling, analysis and management for microprocessors and platform levels for high-performance computing systems. The first paper proposes co-optimization of fan-speed with chip level frequency/voltage for overall energy efficiency. The second paper analyses through-Si-vias and microfluidic cooling as possible thermal solutions. The third paper illustrates the use of electrical models for computing interconnect temperatures in chip microprocessors.

8B.1 MULTI-FUNCTIONAL INTERCONNECT CO-OPTIMIZATION FOR FAST AND RELIABLE 3D STACKED ICs

Young-Joon Lee (yjlee@ece.gatech.edu), Rohan Goel, Sung Kyu Lim - *Georgia Institute of Technology*

8B.2 ENERGY-OPTIMAL DYNAMIC THERMAL MANAGEMENT FOR GREEN COMPUTING

Donghwa Shin (dshin@elpl.snu.ac.kr), Jihun Kim - *Seoul National Univ.*

Jinhang Choi, Sung Woo Chung - *Korea Univ.*

Eui-Young Chung - *Yonsei Univ.*

Naehyuck Chang - *Seoul National Univ.*

8B.3 FAST 3-D THERMAL ANALYSIS OF COMPLEX INTERCONNECT STRUCTURES USING ELECTRICAL MODELING AND SIMULATION METHODOLOGIES

Chuan Xu (chuanxu@ece.ucsb.edu) - *Univ. of California, Santa Barbara*

Lijun Jiang - *IBM T.J. Watson Research Center*

Seshadri K. Kolluri - *Univ. of California, Santa Barbara*

Barry J. Rubin, Alina Deutsch - *IBM T.J. Watson Research Center*

Howard Smith - *IBM Corp.*

Kaustav Banerjee - *Univ. of California, Santa Barbara*

Time: 8:30 AM - 10:00 AM

Room: Pine

SESSION 8C • ANALYTIC PLACEMENT

Moderator: Bill M. Halpin - *Synopsys, Inc.*

This session presents several extensions of analytic placement. The first paper considers the voltage drop problem, shifting logic elements towards power lines, and avoiding power hotspots. The second paper considers three-dimensional placement and studies the impact of through-silicon vias. The final paper reimplements an analytic placer to run on commodity graphics co-processors, obtaining a speedup with a slight deterioration of results.

8C.1 B VOLTAGE-DROP AWARE ANALYTICAL PLACEMENT BY GLOBAL POWER SPREADING FOR MIXED-SIZE CIRCUIT DESIGNS

Yi-Lin Chuang (nicky@eda.ee.ntu.edu.tw), Po-Wei Lee, Yao-Wen Chang - *National Taiwan Univ.*

8C.2 A STUDY OF THROUGH-SILICON-VIA IMPACT ON THE 3-D STACKED IC LAYOUT

Dae Hyun Kim (daehyun@ece.gatech.edu), Krit Athikulwongse, Sung Kyu Lim - *Georgia Institute of Technology*

8C.3 PARALLEL MULTI-LEVEL ANALYTICAL GLOBAL PLACEMENT ON GRAPHICS PROCESSING UNITS

Jason Cong, **Yi Zou** (zouyi@cs.ucla.edu) - *Univ. of California, Los Angeles*

Time: 8:30 AM - 10:00 AM

Room: Cedar

SESSION 8D • PERFORMANCE AND POWER ISSUES IN EMBEDDED SYSTEM-LEVEL DESIGN

Moderators: **Alessandro Pinto** - *United Technologies Corp.*
Luca Carloni - *Columbia Univ.*

This session presents advances to optimize performance and power in various classes of embedded systems.

The first paper introduces a methodology to optimize the organization of high-bandwidth memory subsystems for extensible processors.

The second paper proposes an automatic memory partitioning technique to improve data processing throughput and reduce power consumption of pipelined loop kernels in embedded applications.

The third paper addresses the problem of optimally assigning different battery packs to each node of a heterogeneous wireless sensor network to maximize its lifetime.

8D.1 MEMORY ORGANIZATION AND DATA LAYOUT FOR INSTRUCTION SET EXTENSIONS WITH ARCHITECTURALLY VISIBLE STORAGE

Panagiotis Athanasopoulos (panagiotis.athanasopoulos@epfl.ch), Philip Brisk, Yusuf Leblebici, Paolo Ienne - *Ecole Polytechnique Federale de Lausanne*

8D.2 AUTOMATIC MEMORY PARTITIONING AND SCHEDULING FOR THROUGHPUT AND POWER OPTIMIZATION

Jason Cong, **Wei Jiang** (wjiang@cs.ucla.edu), Bin Liu, Yi Zou - *Univ. of California, Los Angeles*

8D.3 BATTERY ALLOCATION FOR WIRELESS SENSOR NETWORK LIFETIME MAXIMIZATION UNDER COST CONSTRAINTS

Hengyu Long (longhy03@mails.tsinghua.edu.cn), Yongpan Liu, Yiqun Wang - *Tsinghua Univ.*
Robert P Dick - *Univ. of Michigan*
Huazhong Yang - *Tsinghua Univ.*

All speakers are denoted in bold
S - denotes short paper
B - denotes best paper candidate

Wednesday, November 4, 2009

Time: 8:30 AM - 10:00 AM

Room: Donner

SESSION 8E • TUTORIAL: BIOLOGICAL CIRCUITS AND SYSTEMS

This tutorial explores some parallels between circuits and systems in electronics, and those in biology. In particular, this tutorial takes a detailed look at two areas that appear to have close parallels to electronic circuits. The first is gene regulatory networks, or genetic circuits, while the second is networks of the nervous system, or neural circuits. The first problem in discovering these parallels is that each field has its own language and fundamental concepts. Therefore, for each of application area, we first give a brief introduction, tuned for design automation researchers, of the biological knowledge necessary to understand these circuits. Next, an overview is given of the methods that are currently employed in modeling, analysis, and even design in the case of genetic circuits. We believe that there are many parallels (but also many differences) to the techniques employed for the analysis of electronic circuits. Therefore, our hope is that this tutorial will help design automation researchers see their potentially important role that they have to play in systems and synthetic biology research.

Presenters: **Chris J. Myers** - *Univ. of Utah*
Lou Scheffer - *Janelia Farms, Howard Hughes Medical Institute*

8E.1 GENETIC DESIGN AUTOMATION

Chris J. Myers - *Univ. of Utah*
Nathan Barker - *Southern Utah Univ.*
Kevin Jones - *Univ. of Utah*
Hiroyuki Kuwahara - *Carnegie Mellon Univ.*
Curtis Madsen - *Univ. of Utah*
Nam-Phuong Nguyen - *Univ. of Texas, Austin*

Time: 10:30 AM - 12:00 PM

Room: Oak

SESSION 9A • STATISTICAL SIMULATION AND OPTIMIZATION OF SERIAL LINK AND WORDLENGTH

Moderator: Eli Chiprout - *Intel Corp.*

The first paper in this session introduces a statistical simulation for serial links, and the second paper presents a joint design-time and post-silicon optimization for digitally tunned analog circuits including serial links. The last two papers optimize word length for DSP and datapath applications.

9A.1 AN ELECTRICAL-LEVEL SUPERPOSED-EDGE APPROACH TO STATISTICAL SERIAL LINK SIMULATION

Michael Tsuk (mtsuk@ansoft.com), Daniel Dvorscak, Chin Siong Ong - *Ansoft LLC*
Jacob White - *Massachusetts Institute of Technology*

9A.2 JOINT DESIGN-TIME AND POST-SILICON OPTIMIZATION FOR DIGITALLY TUNED ANALOG CIRCUITS

Wei Yao, Yiyu Shi, **Lei He** (lhe@ee.ucla.edu), Sudhakar Pamarti - *Univ. of California, Los Angeles*

9A.3 FAST TRADE-OFF EVALUATION FOR DIGITAL SIGNAL PROCESSING SYSTEMS DURING WORDLENGTH OPTIMIZATION

Linsheng Zhang (zhanglinsheng@gmail.com), Yan Zhang, Wenbiao Zhou - *Harbin Institute of Technology*

9A.4 IMPROVED HEURISTICS FOR FINITE WORD-LENGTH POLYNOMIAL DATAPATH OPTIMIZATION

Bijan Alizadeh, **Masahiro Fujita** (fujita@ee.t.u-tokyo.ac.jp) - *VLSI Design and Education Center, CREST and Univ. of Tokyo*

Time: 10:30 AM - 12:00 PM

Room: Fir

SESSION 9B • PARASITIC EXTRACTION, MODELING, AND REDUCTION TECHNIQUES

Moderator: Zhenhai Zhu - *Cadence Design Systems, Inc.*

This session begins with a paper that describes techniques for decap-aware placement to reduce power supply noise. The next paper describes an efficient 3-D capacitance extraction approach based on a hierarchical floating random walk technique. The next three papers describe recent advances in parasitic model order reduction. The first paper in this category describes a parametric macromodeling technique based on a vector-fitting algorithm. The next paper proposes a generalized Hamiltonian method for model order reduction. The final paper describes techniques for fast and reliable passivity assessment based on an extended Hamiltonian pencil formulation.

9B.1 DECOUPLING CAPACITANCE EFFICIENT PLACEMENT FOR REDUCING TRANSIENT POWER SUPPLY NOISE

Xiaoyi Wang (wangxiaoyi00@gmail.com), Yici Cai, Qiang Zhou - *Tsinghua Univ.*

Sheldon X.-D. Tan, Thom Eguia - *Univ. of California, Riverside*

9B.2 B A HIERARCHICAL FLOATING RANDOM WALK ALGORITHM FOR FABRIC-AWARE 3-D CAPACITANCE EXTRACTION

Tarek A. El-Moselhy (tmoselhy@mit.edu) - *Massachusetts Institute of Technology*

Ibrahim M. Elfadel - *IBM Corp.*

Luca Daniel - *Massachusetts Institute of Technology*

9B.3 ACTIVE-PASSIVE CO-SYNTHESIS OF MULTI-GIGAHERTZ RADIO FREQUENCY CIRCUITS WITH BROADBAND PARAMETRIC MACROMODELS OF ON-CHIP PASSIVES

Ritochit Chakraborty (ritochit@u.washington.edu), Arun V. Sathar-nur, Vikram Jandhyala - *Univ. of Washington*

9B.4S GHM: A GENERALIZED HAMILTONIAN METHOD FOR PASSIVITY TEST OF IMPEDANCE/ADMITTANCE DESCRIPTOR SYSTEMS

Zheng Zhang (zzhang@eee.hku.hk), Ngai Wong, Chi-Un Lei - *The Univ. of Hong Kong*

9B.5S FAST AND RELIABLE PASSIVITY ASSESSMENT AND ENFORCEMENT WITH EXTENDED HAMILTONIAN PENCIL

Zuochang Ye (zuochang@tsinghua.edu.cn) - *Tsinghua Univ.*

Luis Miguel Silveira - *INESC ID, Cadence Research Labs and IST/TU Lisbon*

Joel R. Phillips - *Cadence Design Systems, Inc.*

WORKSHOP RECEPTION

WEDNESDAY, NOVEMBER 4 IN THE GATEWAY FOYER

5:30 - 6:30pm

All speakers are denoted in bold
S - denotes short paper
β - denotes best paper candidate

Wednesday, November 4, 2009

Time: 10:30 AM - 12:00 PM

Room: Pine

SESSION 9C • ADVANCED BOOLEAN TECHNIQUES IN LOGIC SYNTHESIS

Moderators: Satrajit Chatterjee - *Intel Corp.*
Alan Mishchenko - *Univ. of California, Berkeley*

This session includes four papers describing new Boolean techniques and their application to Logic Synthesis. The first paper presents efficient techniques to determinize a Boolean relation. The second paper uses logical implications to detect node merging opportunities during circuit restructuring. The third paper presents an industry-strength logic difference optimizer for ECOs. The last paper presents a new approach to optimize arithmetic circuits by reasoning about the information flow in the arithmetic operation.

9C.1 INTERPOLATING FUNCTIONS FROM LARGE BOOLEAN RELATIONS

Jie-Hong R. Jiang, Hsuan-Po Lin, **Wei-Lun Hung**
(b91076@csie.ntu.edu.tw) - *National Taiwan Univ.*

9C.2 FAST DETECTION OF NODE MERGERS USING LOGIC IMPLICATIONS

Yung-Chih Chen, **Chun-Yao Wang** (wcyao@cs.nthu.edu.tw) - *National Tsing-Hua Univ.*

9C.3 DELTASYN: AN EFFICIENT LOGIC-DIFFERENCE OPTIMIZER FOR ECO SYNTHESIS

Smita Krishnaswamy (krishnaswamy.smita@gmail.com),
Haoming Ren - *IBM T.J. Watson Research Center*
Nilesh Modi - *Univ. of California, Santa Barbara*
Ruchir Puri - *IBM T.J. Watson Research Center*

9C.4 ITERATIVE LAYERING: OPTIMIZING ARITHMETIC CIRCUITS BY STRUCTURING THE INFORMATION FLOW

Ajay K. Verma, **Philip Brisk** (philip.brisk@epfl.ch), Paolo lenne - *Ecole Polytechnique Federale de Lausanne*

Time: 10:30 AM - 12:00 PM

Room: Pine

SESSION 9D • TUTORIAL: GLOBAL ROUTING REVISITED

Moderators: Satrajit Chatterjee - *Intel Corp.*
Alan Mishchenko - *Univ. of California, Berkeley*

In this embedded tutorial, we visit (and revisit) the topic of global routing. We provide a brief review of global routing's history, and touch on recent work that has contributed to the state-of-the-art in the field. While we cover in depth the basic principles behind modern approaches to the problem, we also emphasize open challenges and real problems that remain unresolved. We argue that not only does the current academic formulation lack key components of the true routing problem -- such as scenic control, layer directives, and capabilities for integration with physical synthesis -- but also that present methods are likely to fail when extended toward the more generalized formulation. Finally, we plan to release a revision of the ISPD benchmarks (augmented with a richer family of routing directives) to encourage continued progress in the research community.

Presenter: **Michael D. Moffitt** - *IBM Corp.*

Time 8:30AM - 6:00PM - Room: Donner

COLOCATED WORKSHOP: **CIRCUIT AND MULTI-DOMAIN SIMULATION WORKSHOP (CMS)**

Organizers: Peng Li - *Texas A&M Univ.*
Luis Miguel Silveira - *INESC ID, Cadence Research Labs and IST/TU Lisbon*
Peter Feldmann - *IBM T.J. Watson Research Center*

Simulation is a fundamental technique that facilitates understanding, analysis and design of an extremely broad range of circuits and systems, including integrated electronic circuits, other types of electrical systems, and mechanical, chemical and biological networks. While a wealth of methods have evolved to serve a vast body of applications, there is an unsaturated demand for delivering higher accuracy, faster speed and novel analysis capabilities with the increase of design complexity, necessities in capturing increasingly complex device and system behaviors, and facilitating more efficient design verification and optimization. There exist significant challenges in developing simulation algorithms and implementations that deliver required efficiency and robustness across a wide spectrum of circuit/system types and at different levels of hierarchy. To address such challenges, it is likely that innovations in fundamental algorithm development, novel application of modeling techniques and paradigms shifts in implementation methodologies are required.

This workshop provides a forum for showcasing the latest developments and practices in simulation, interpreted in a broad sense, and covers topics such as (but not limited to):

- SPICE/Analog/RF simulation algorithms
- Techniques for analyzing and verifying IC power grids
- Smart grids and energy efficiency
- System-level simulation and modeling of large interconnected networks
- Modeling and simulation for emerging nano and bio applications
- Advanced device modeling and its implications on circuit simulation
- Massively parallel circuit simulation
- Formal and semi-formal analog verification
- Theory and practice of Fast SPICE
- Model order reduction

More details of the workshop may be found at:
<http://www.ece.tamu.edu/~pli/cms>

Presenters: Prateek Bhansali - *Univ. of California, Berkeley*
Eli Chiprout - *Intel Corp.*
Roland Freund - *Univ. of California, Davis*
Lars Hedrich - *Frankfurt Univ.*
Marija Ilic - *Carnegie Mellon Univ.*
Eric Keiter - *Sandia National Labs*
Ken Kundert - *Designer's Guide Consulting*
Peng Li - *Texas A&M Univ.*
Elebeoba May - *Sandia National Labs*
Bruce W. McGaughey - *ProPlus Design Solutions*
Michal Rewienski - *Synopsys, Inc.*
Heidi Thornquist - *Sandia National Labs*
Jacob White - *Massachusetts Institute of Tech.*

Co-Sponsored by:



Physical Design Technical Committee

Time 8:00AM - 5:00PM - Room: Siskiyou

COLOCATED WORKSHOP: **WORKSHOP ON VARIABILITY MODELING AND CHARACTERIZATION**

Organizers: Yu Cao - *Arizona State Univ.*
Frank Liu - *IBM Corp.*
Hidetoshi Onodera - *Kyoto Univ.*
Dennis Sylvester - *Univ. of Michigan*

It is widely recognized that process variation is emerging as a fundamental challenge to IC design in scaled CMOS technology; and it will have profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, the industry is starting to accept the fact that some of the effects are better mitigated during the design process. Handling variability in the design process will require accurate and appropriate models of variability and its dependence on designable parameters (i.e. layout), and its spatial and temporal distributions. It also requires carefully designed test structures and proper statistical data analysis methods to extract meaningful models from large volumes of silicon measurements. The resulting compact modeling of systematic, random, spatial, and temporal variations is essential to abstract the physical level variations into a format the designers (and more importantly, the tools they use) can utilize. This workshop provides a forum to discuss current practice as well as near future research needs in test structure design, variability characterization, compact variability modeling, and statistical simulation.

Key topics of this workshop includes (but not limited to):

- Physics mechanisms and technology trends of device-level variations
- First-principles simulation methods for predicting variability
- Time-dependent variation and their interaction with other variation sources
- Compact modeling of variations in transistors and interconnect
- Device and circuit level modeling techniques
- Test structure design for variability
- Variability characterization and bounding
- Statistical data analysis and model extraction methods
- Novel implementation and simulation techniques for dealing with variability

Workshop website: <http://www.eas.asu.edu/~ycao/cvm/>

Presenters: **Scott Roy** - *Univ. of Glasgow*
Vikas Chandra - *ARM Ltd.*
Larry Clark - *Arizona State Univ.*
Abe Elfadel - *IBM Corp.*
Puneet Gupta - *Univ. of California, Los Angeles*
Chris Kim - *Univ. of Minnesota*
Xin Li - *Carnegie Mellon Univ.*
Tsu-Jae King Liu - *Univ. of California, Berkeley*
Victor Moroz - *Synopsys, Inc.*
Paul Newman - *Intel Corp.*
Tanya Nigam - *GlobalFoundries*
Naoki Tega - *Hitachi America, Ltd.*

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Please join us for a unique event with Martin Davis, the recipient of this year's SIGDA Pioneering Achievement Award for his outstanding contributions to algorithms for solving the Boolean Satisfiability problem, which heavily influenced modern tools for hardware and software verification, as well as logic synthesis.



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