DVCon is the premier conference on the application of languages, tools, and methodologies for the design and verification of electronic systems and integrated circuits. The focus of the conference is the usage of specialized design and verification languages such as SystemVerilog, Verilog, VHDL, PSS, SystemC and e, as well as general purpose languages such as C, C++, Python, PERL and Tcl. Tools and methodologies include the use of machine learning, open-source software, hardware and architecture, testbench automation, hardware-assisted verification, hardware/software co-verification, formal verification, functional safety and security, transaction-level system design, high-level synthesis, low power design techniques, 3D chip designs, IP-based SoC design methods, reference flows and AMS design and verification.

DVCon is seeking tutorial topics that are current, have a high-level of interest and offer strong continuing educational content.

Tutorial sponsors reach a captive audience during the 3 hrs of educational sessions and have the opportunity to follow-up with them during breaks, at the exhibits, and following the event.

DVCon is a highly targeted venue for engineers addressing major design and verification issues. You can position your company at the forefront of these discussions by sponsoring either of the Tutorials listed below. Submit proposals by Tuesday, September 14. For suggested topics and timeline, see page 2.

**DVCON SPONSORED TUTORIAL WITH LUNCHEON: $18,500**

Sponsorship Includes:

- Complimentary 8x10 booth on the Exhibit Floor
- 3-hour technical presentation
- Individualized luncheon, including opportunity to present company-specific content to luncheon attendees
- Ability to collect contact information from the Sponsored Luncheon attendees
- Copy of the 2020 Attendee Lists (no email addresses)
- Copy of the Sponsored Tutorial Attendee List (email addresses included)
- Tutorial and Luncheon content will be publicized via monthly newsletters, DVCon website, Conference Program and in the Opening Session presentation slides
- 1 dedicated email distribution to the DVCon mail list
- Other promotional items like banners, flyers, gift items, etc. can be distributed at these two events
- Presenters for the tutorial and lunch are entitled to a complimentary one-day registration
- Up to 10 complimentary one-day registrations for the tutorial and lunch presentation

*Sponsored tutorials will be reviewed and approved by the program committee with respect to technical depth and applicability. In case of multiple organizations presenting a sponsored tutorial only the organizing company would get the sponsorship benefits mentioned above.*

For more information concerning the conference, please contact the conference management, Laura LeBlanc at lleblanc@conferencecatalysts.com

Detailed guidelines for preparing the presentations will be made available after selections are final.
DVCon tutorials are open to all attendees and are included in the full conference registration. Please include in the proposal the name of the companies that will be sponsoring the tutorial.

- Attendee expectations are high regarding currency of topic, depth of engineering content and breadth of real-life examples
- The Tutorial Chair will review final presentation materials to ensure high quality educational content
- Include suggested presenters names, affiliations & biographies
- Your proposal should be a short abstract of the tutorial, two to five paragraphs, 1,000 words maximum

Presentation slides need to be supplied in an electronic format in advance of the conference. Presentation slides will be distributed to the attendees in electronic format. Hard copies will not be provided

- Please indicate if this tutorial is a “hands-on” session or lecture format
- Any necessary additional hardware that you may require must be provided by the tutorial organizers

SUGGESTED TOPICS

DVCon tutorials are open to all attendees and are included in the full conference registration. Please include in the proposal the name of the companies that will be sponsoring the tutorial.

- SystemVerilog for Verification and/or Design
- SystemC/C/C++ Design and/or Verification of systems.
- SoC and Software-driven Verification
- Assertion-based Verification. SystemVerilog Assertions, PSL, etc.
- Coverage-driven Verification
- High-level Synthesis
- Low-power Design and Verification techniques
- Secure/Encrypted IP-based SoC design methods
- Debug for design and verification
- Mixed-signal modeling and verification
- Transaction Level Modeling (TLM), ESL Design, and IP integration (IP-XACT)
- Functional Safety
- Security
- Embedded software verification
- Hardware/Software Co-development
- Verification Productivity Methods
- Formal Methodology and Static Analysis
- Emulation
- Post SI Debug
- FPGA Prototyping
- Moving from proprietary solutions to standards-based design and verification
- Portable Stimulus
- Application-specific design verification challenges and techniques
- Machine Learning applications for verification and design
- Open source hardware/software/architecture

TUTORIAL DEADLINES

- September 14, 2021: Proposals due. Submit at DVCon.org
- October 26, 2021: Accept/Reject notification
- November 17, 2021: All Tutorial content due for Conference Program and website: tutorial title, abstract, speaker names, affiliations and biographies
- January 4, 2022: Draft Presentation slides due to DVCon Tutorial Chair
- January 7, 2022: Presentation feedback due to presenters on slides
- January 14, 2022: Final slides due for final production for attendee distribution

CONFERENCE SCHEDULE

- Monday, February 28:
  - Accellera Day Tutorials
  - Short Workshops
  - Exhibits
- Tuesday, March 1:
  - Technical Sessions
  - Keynote Speaker
  - Poster Session
  - Exhibits
- Wednesday, March 2:
  - Technical Sessions
  - Panel Discussions
  - Exhibits
- Thursday, March 3:
  - Tutorials
  - Short Workshops