

Design and verification in ARM



ARM

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General Manager, Technology Services Group, ARM

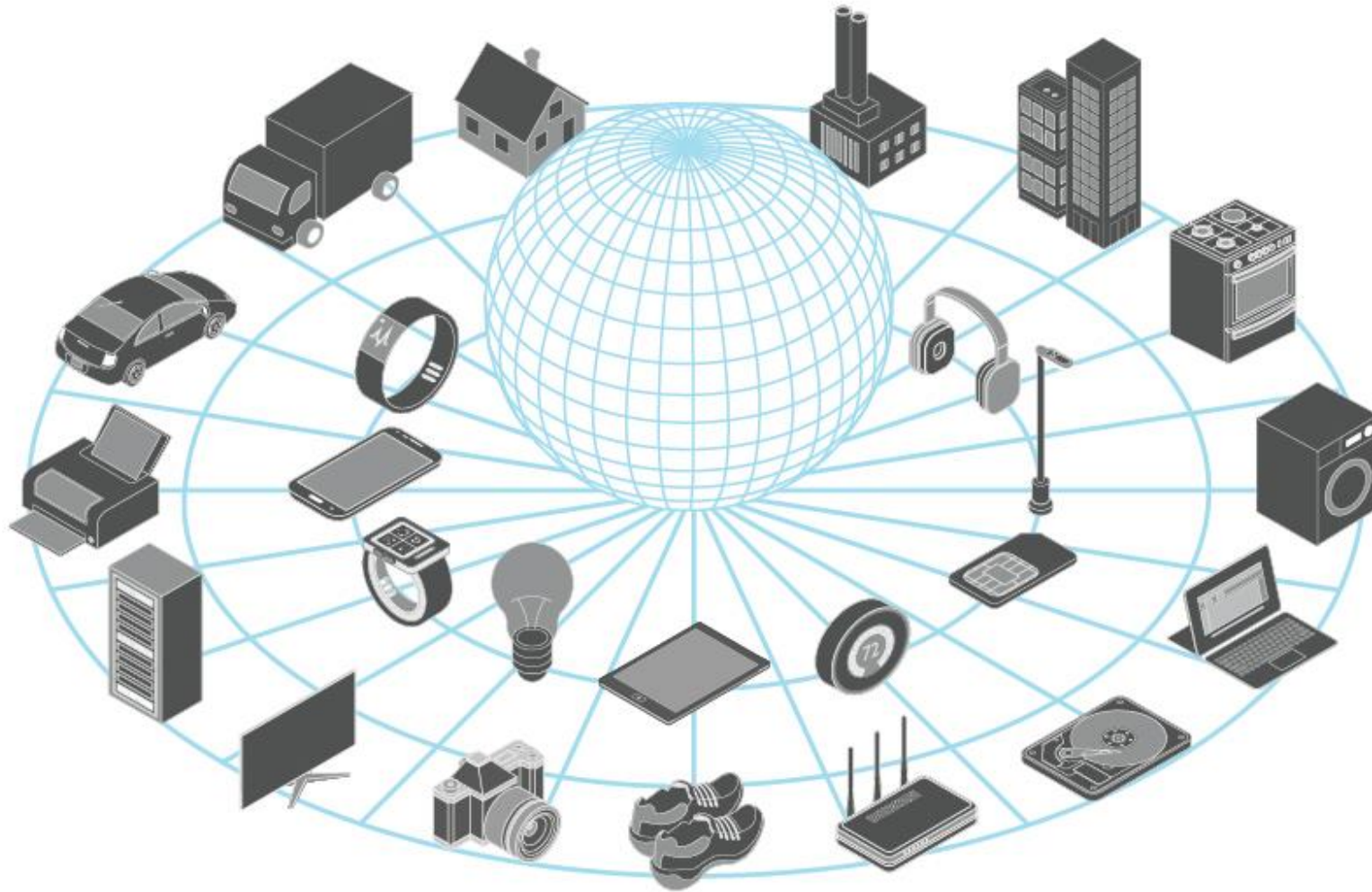
DVCon Europe
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Themes of this presentation

- About ARM
- Insight into design and verification in ARM
 - Technology Services Group
 - Methodology initiatives
- How ARM helps with your design and verification
 - Safety
 - Subsystems
 - New use cases

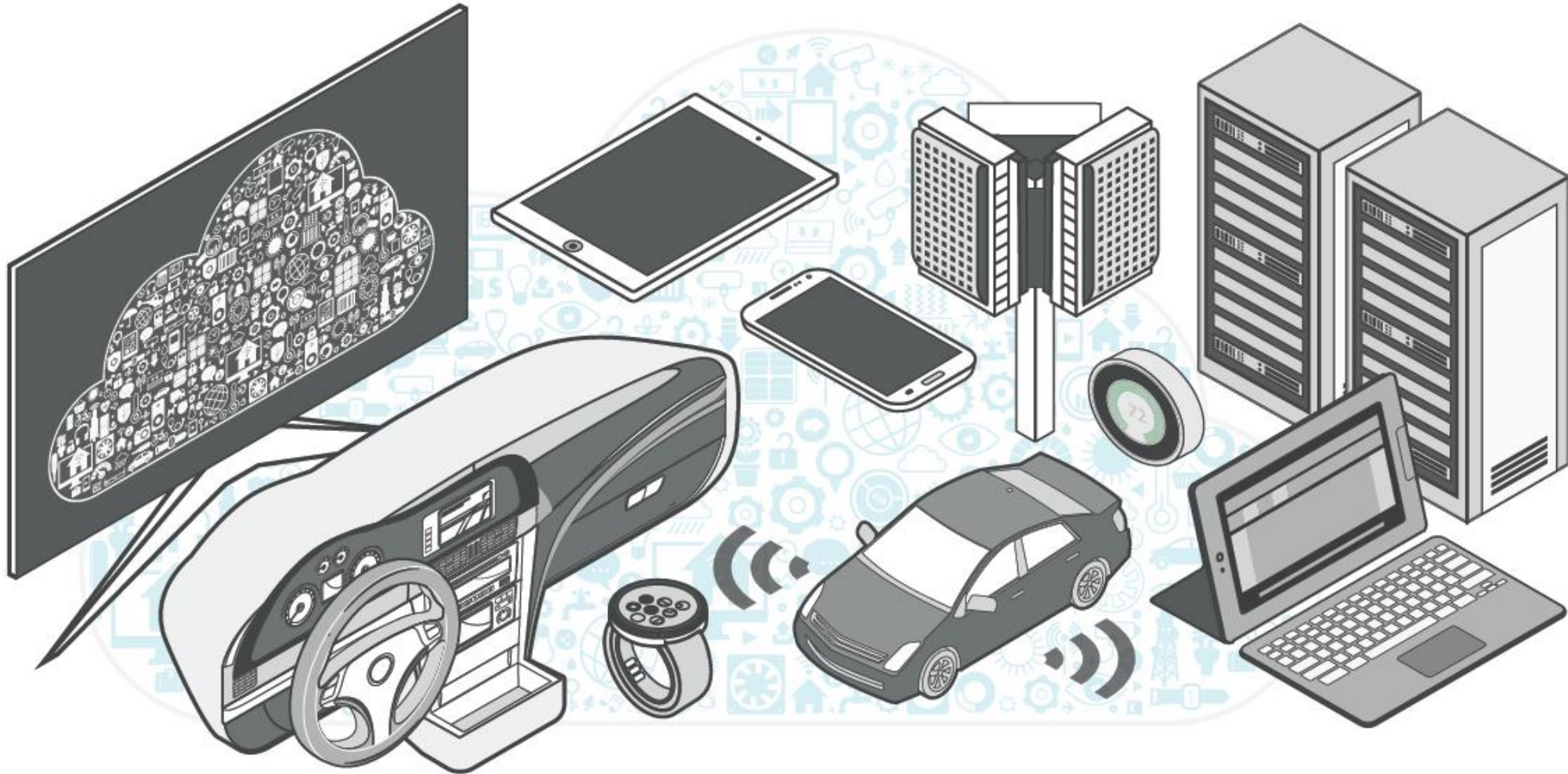
ARM's vision

Technology that invisibly enables opportunity for a globally connected population

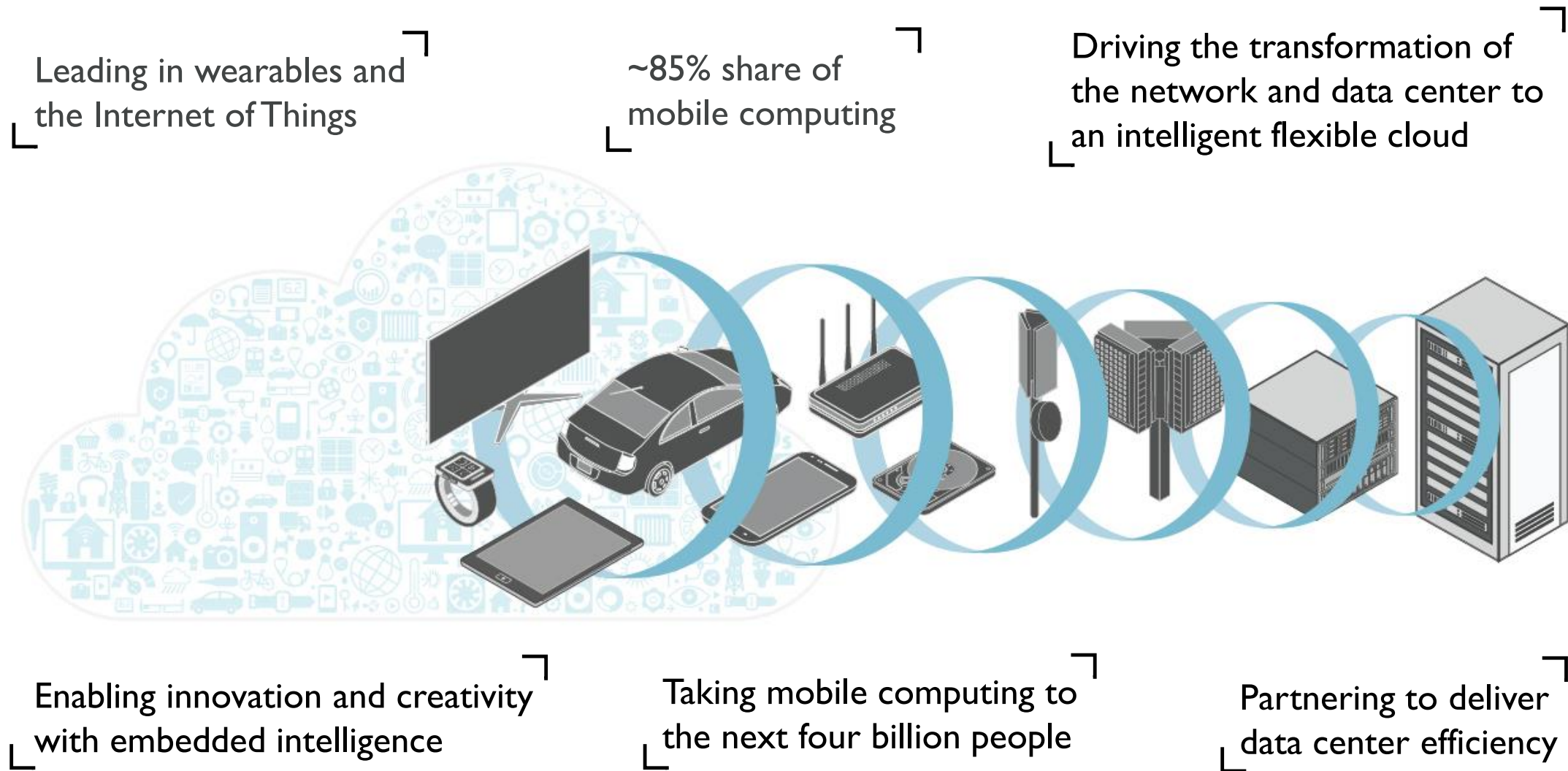


ARM's mission

Deploy energy-efficient ARM-based technology, wherever computing happens...

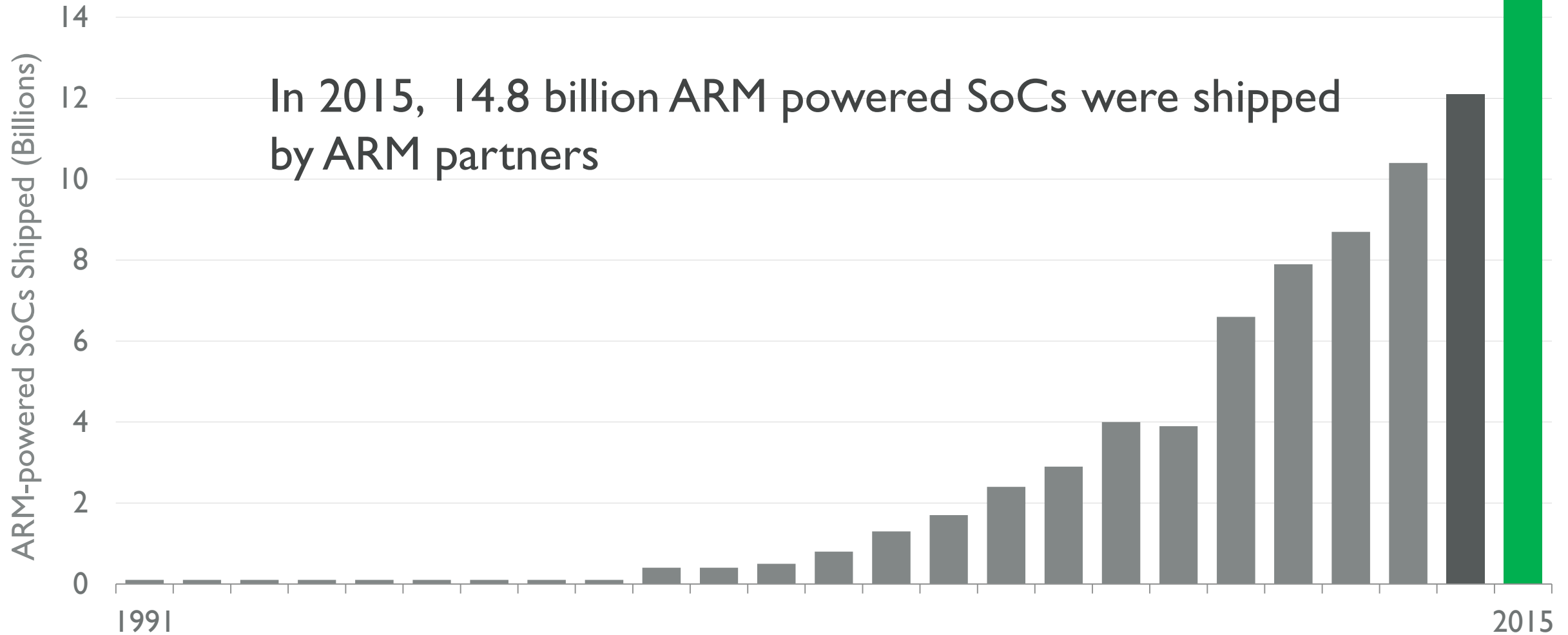


Enabling innovation across the entire industry



ARM partnership: building for the long term

In 2015, 14.8 billion ARM powered SoCs were shipped by ARM partners



ARM partnership: transforming markets

Mobile



Enterprise



Home



Embedded / IoT



ARM technology is increasingly diverse

Advanced consumer products are incorporating more and more ARM technology – from processor and multimedia IP to software

ARM TRUSTZONE

System Security

ARM ARTISAN

Physical IP

ARM MALI

Visual Technology

ARM CORTEX

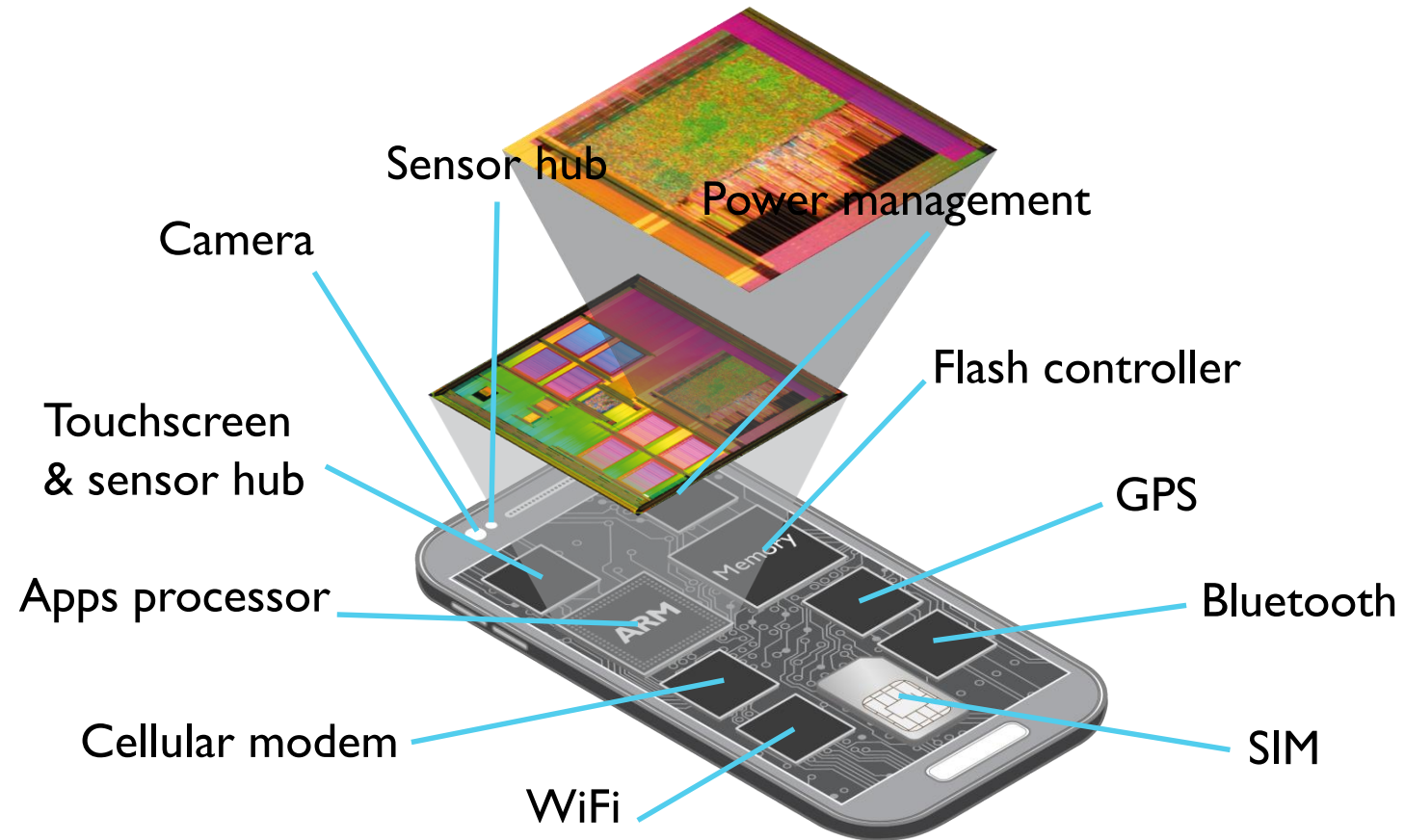
Processor Technology

ARM CORELINK

Processor System IP

ARM CORDIO

Radio Core IP



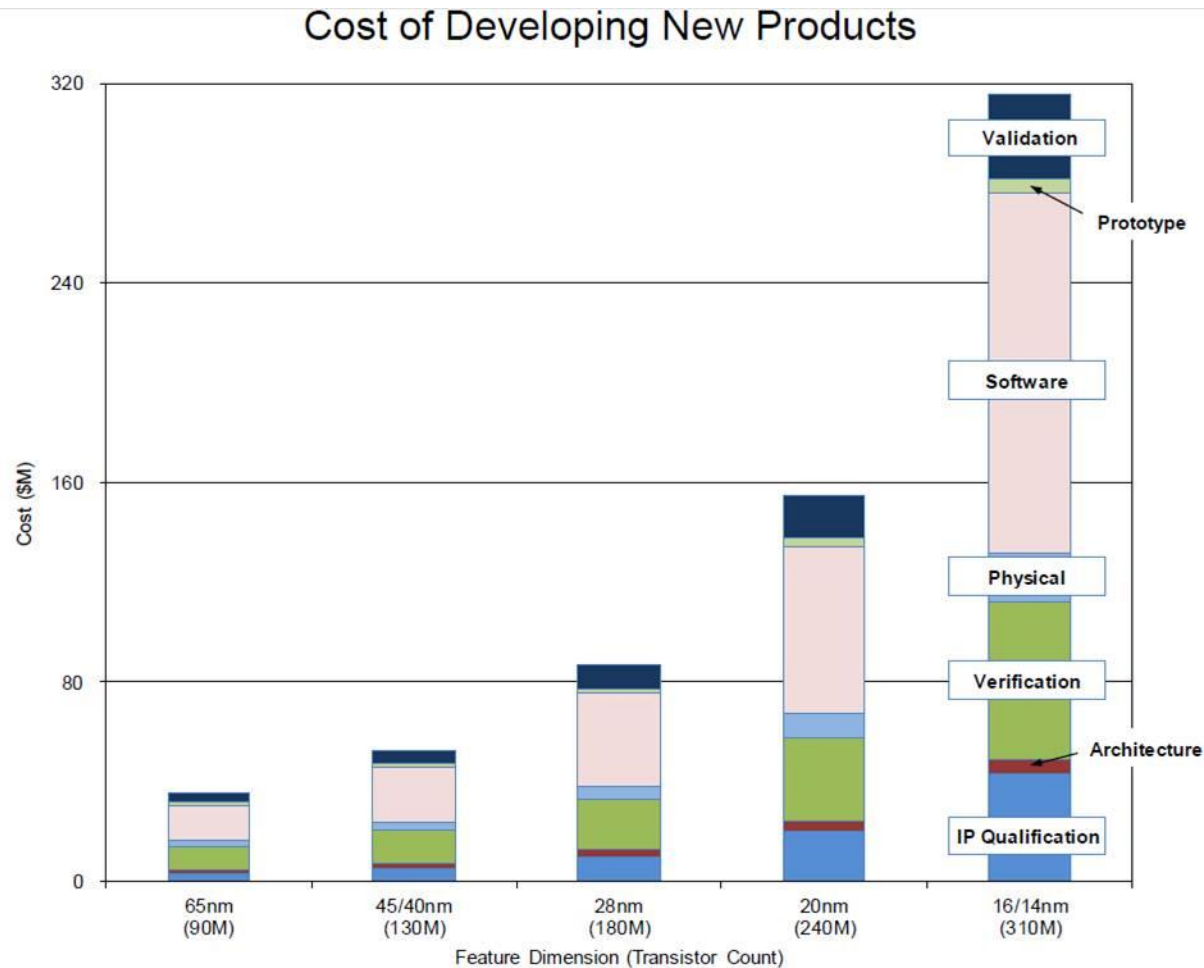
The chip is the system

- ARM delivers technology to drive scalable, efficient system-on-chip (SoC) solutions:
 - **Software** increasing system efficiency with optimized software solutions
 - Diverse components, including **CPUs** and **GPUs** designed for specific tasks
 - **Interconnect System IP** delivering coherency and the quality of service required for lowest memory bandwidth
 - **Physical IP** for a highly optimized processor implementation



And it's getting ever more expensive...

- The cost of developing new SoCs at the leading-edge continues to rise
- We are all experiencing rising infrastructure and tools costs driven by complexity



*“While projections show it will cost as much as \$300 million to develop new SoCs at the leading edge, the real numbers are generally much lower—generally between \$20 million and \$50 million, providing there is plenty of **reusable IP**.”*

ARM internal engineering requirements are demanding

- Thousands of engineers
- Multiple domains and disciplines – CPU, Media, Interconnect, Physical IP, Software...
- Hundreds of optimized, on-chip solutions, with thousands of parts
- Design locations across many continents
- Continuously emerging requirements and growing use cases
- An increasing partner base
- Exponential growth in ARM powered products on the market: **billions** of parts per year

Partners and end customers are ever more dependent on ARM –
we have to do things RIGHT, FIRST TIME!

Complexity drives need for risk mitigation (verification & debug)
= bigger faster compute, better methodologies

Underlying all of this, ARM depends on TSG to enable its own engineering functions

Design and verification in ARM

Technology Services Group

TSG create and operate the platforms, tools and services that:

- enable ARM to create products, and
- promote effectiveness understanding and improvement

We facilitate rather than mandate methodology

Duality: We are engineers and operators, we support and we drive

Novel organisation structure: As an infrastructure team that underpins engineering, we are part of both engineering and the IT department



Technology Services Group

Mission: We create and operate the platforms, tools and services that (a) enable ARM to create products, and (b) promote effectiveness understanding and improvement.

Vision: Our outstanding technology infrastructure and service is a clear differentiator for ARM, helping both Engineering and the Partnership create great products efficiently.

The TSG manifesto: our initiatives to achieve the vision

One ARM: **bridge** across engineering, and between engineering and infrastructure

Support the **shift left** initiatives with a strategy that allows ARM to do more, earlier

Drive and maintain **low power and low waste** DNA

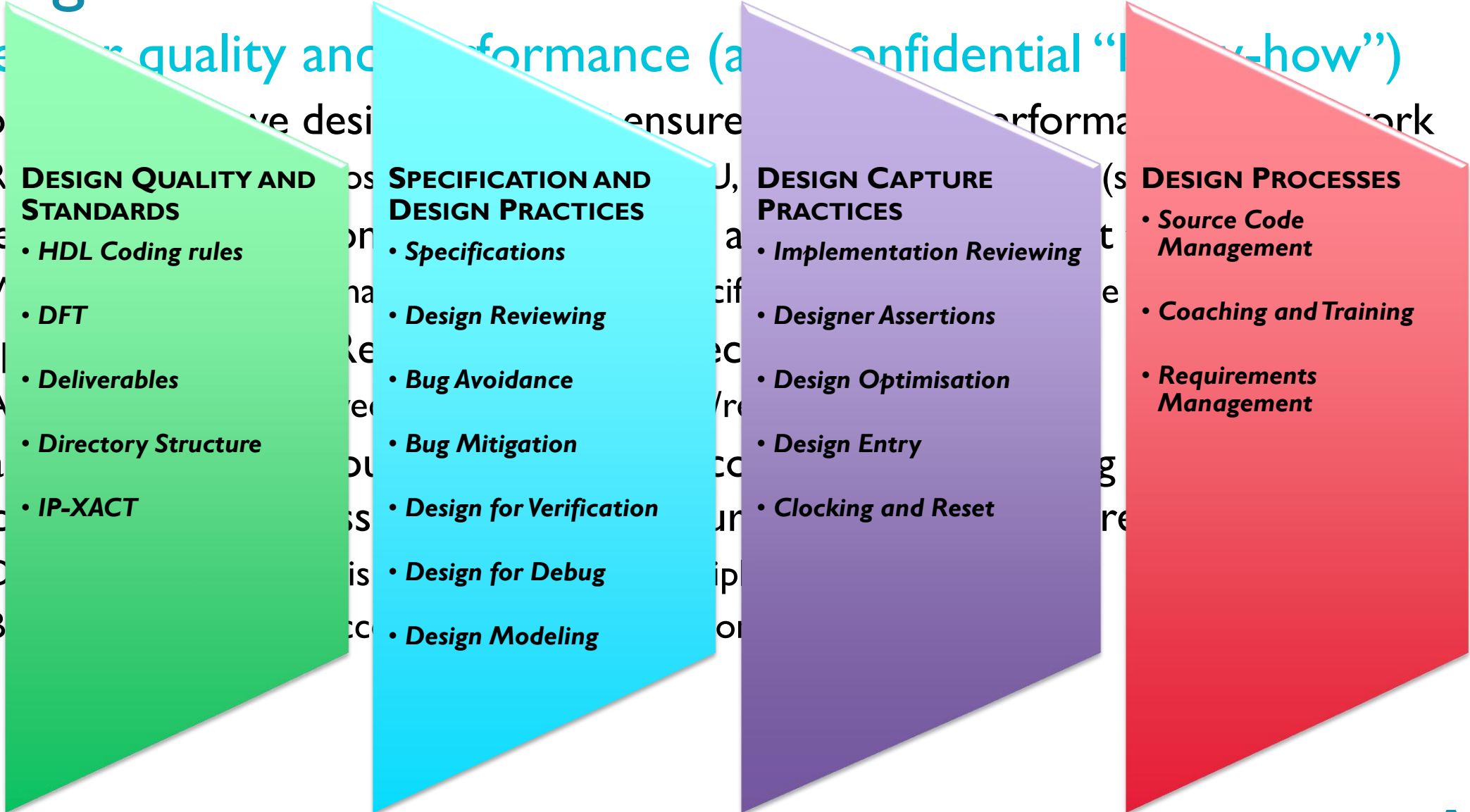
Promote methodology development for **safety critical applications**

Use **big engineering data** and machine learning for design and verification insights

Push into the cloud where practical... ..and the **ARM powered cloud**

Design and verification standards

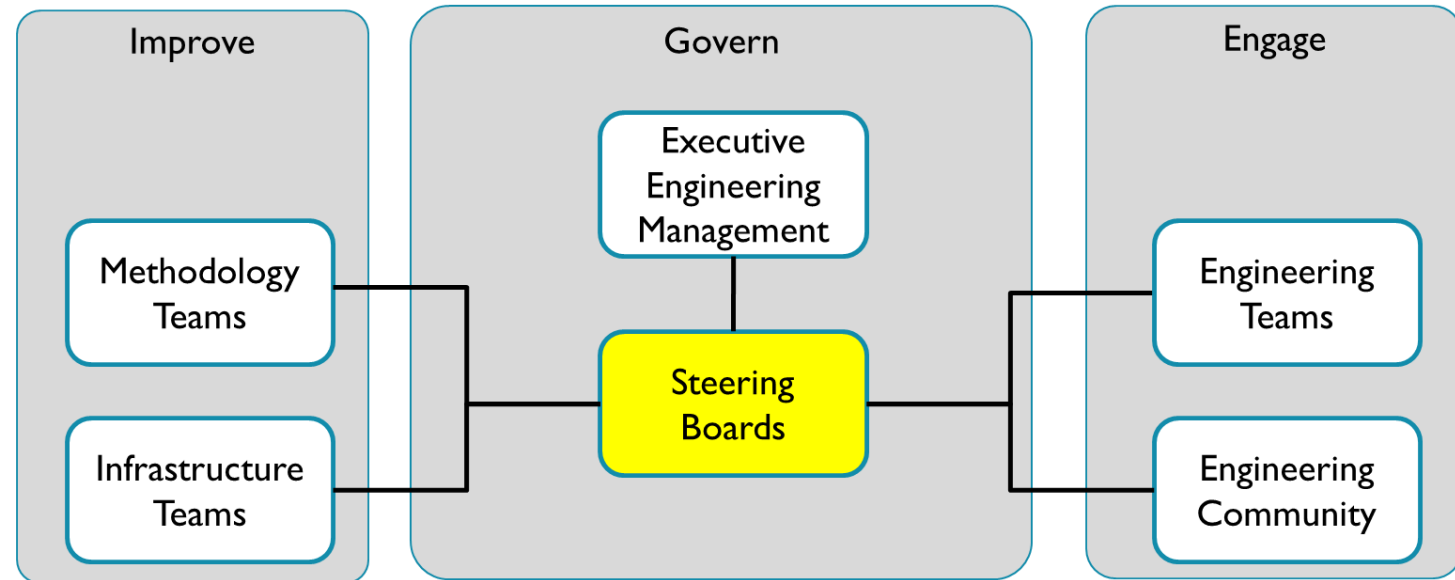
Rules for quality and performance (a confidential “know-how”)

- Comprehensive design ensure performance work
 - R
 - We
 - V
 - Cap
 - A
 - Sta
 - D
 - B
- 
- DESIGN QUALITY AND STANDARDS**
 - HDL Coding rules
 - DFT
 - Deliverables
 - Directory Structure
 - IP-XACT
 - SPECIFICATION AND DESIGN PRACTICES**
 - Specifications
 - Design Reviewing
 - Bug Avoidance
 - Bug Mitigation
 - Design for Verification
 - Design for Debug
 - Design Modeling
 - DESIGN CAPTURE PRACTICES**
 - Implementation Reviewing
 - Designer Assertions
 - Design Optimisation
 - Design Entry
 - Clocking and Reset
 - DESIGN PROCESSES**
 - Source Code Management
 - Coaching and Training
 - Requirements Management

Design and verification steering

- Another challenge in controlling and embracing diversity
- We need structure to steer our infrastructure and methodology work, and make sure it is relevant and right across the breadth of our engineering

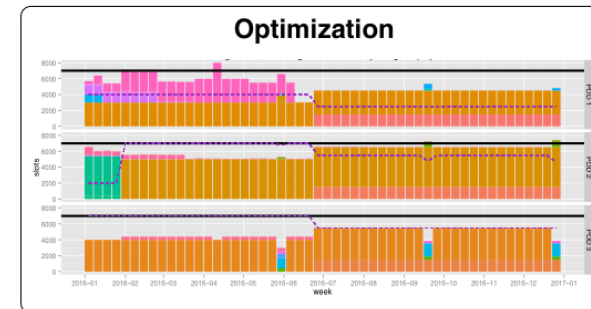
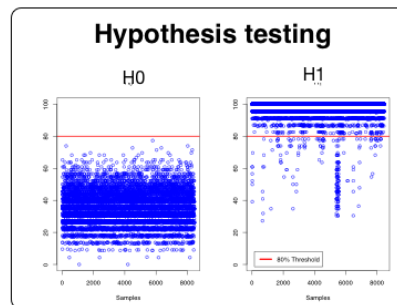
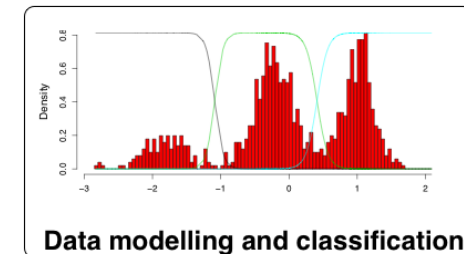
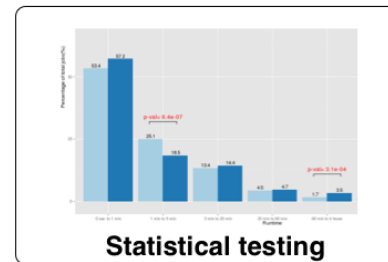
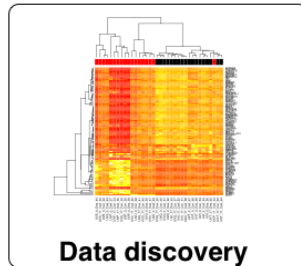
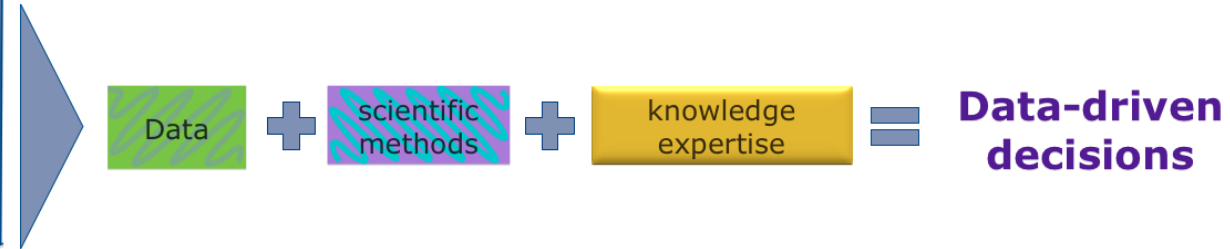
- Our solution is Steering Boards
 - Per domain (e.g., RTL D&V, Simulation, Emulation, Software D&V, Physical Implementation, Physical Characterisation, ...)



- These have become a corner plank of our structure. Not just “talking shops”!

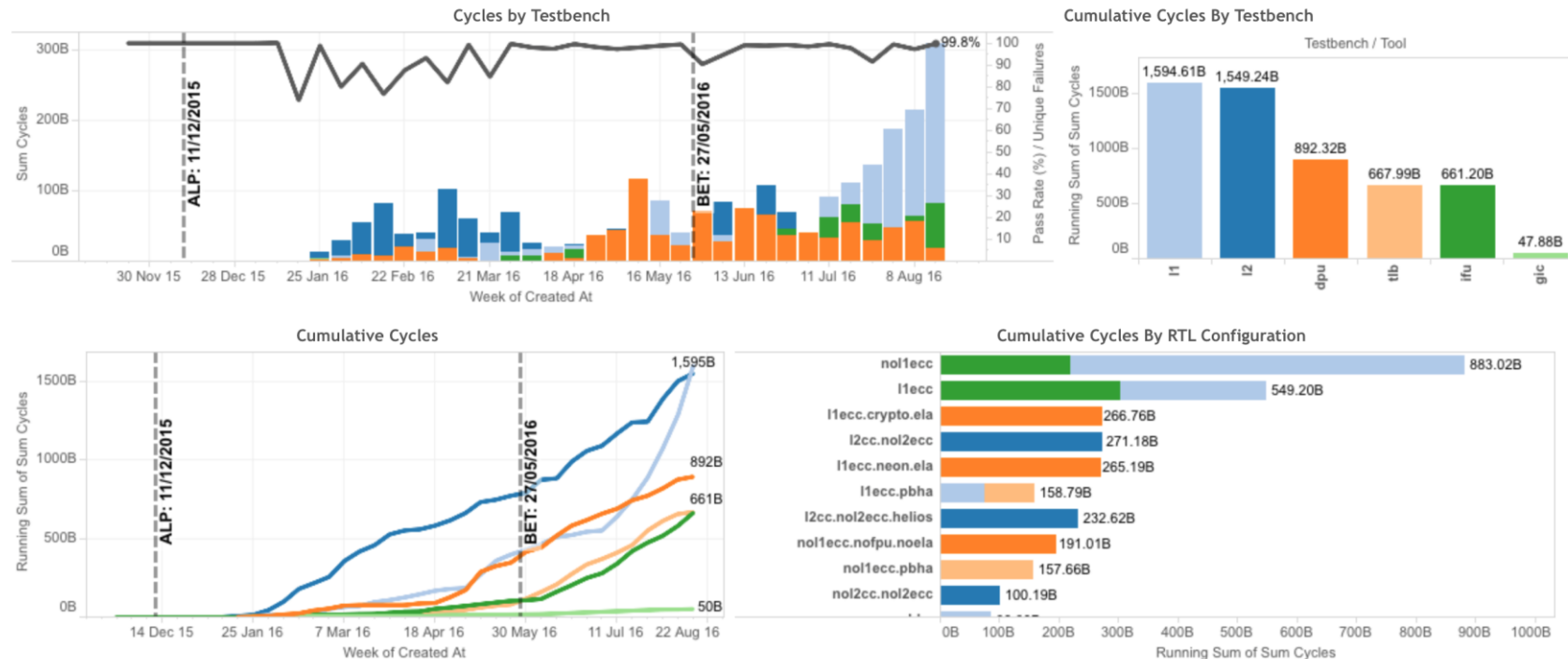
Metrics – analytics driven through data science

Data-intensive science is the extraction of actionable knowledge directly from data through a process of discovery, or hypothesis formulation and hypothesis testing [Gray07].

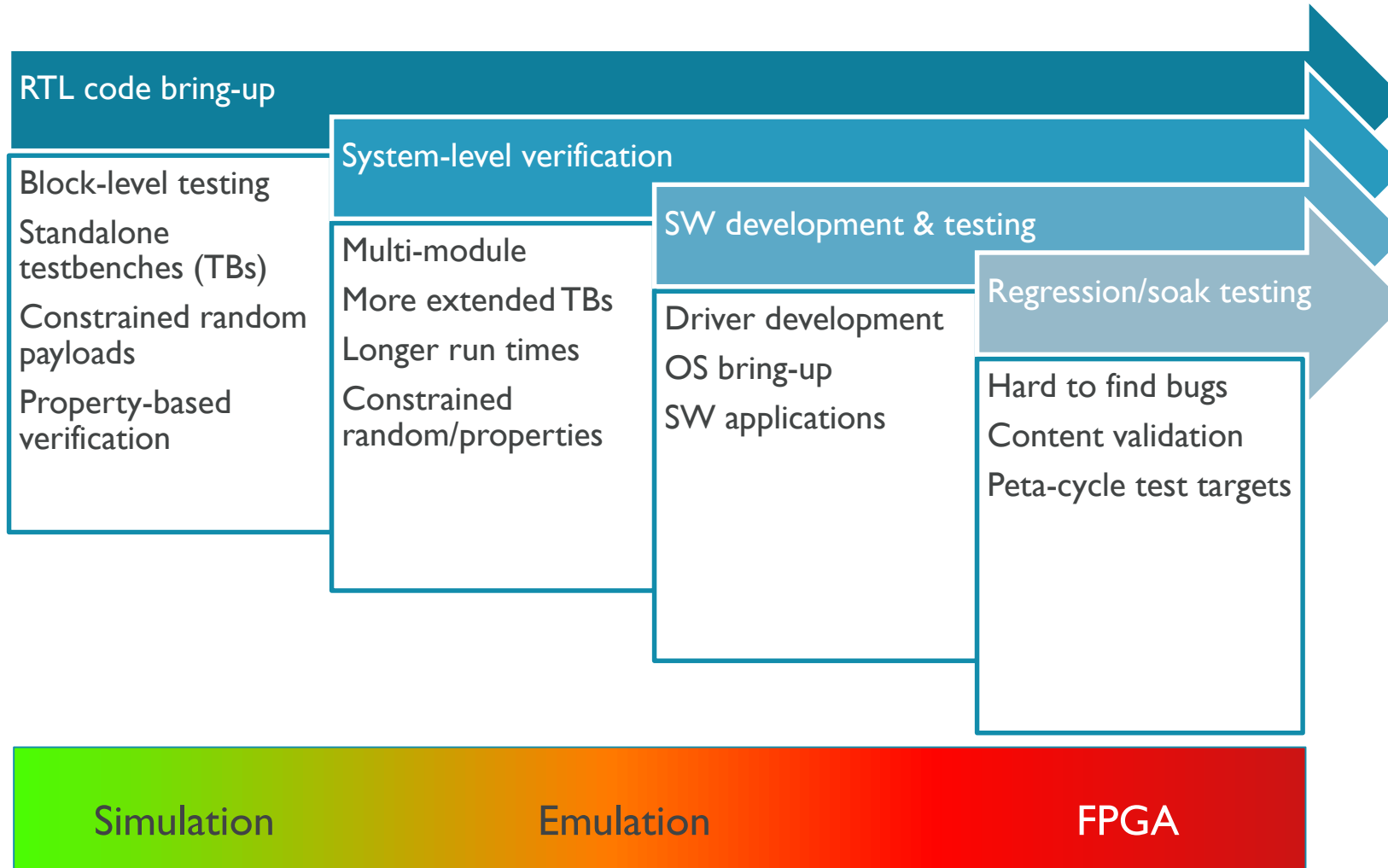


How data science is applied to RTL and verification

- Improved effectiveness through data discovery:
 - Compute, Emulator, FPGA, Verification Results: all profiled together into a single data lake
 - Identification and reduction of ineffective cycles
 - Improved test bench performance in finding more bugs
- Leads to models of IP development for project planning and project improvements
 - Compare across a portfolio of projects, apply science, so projects learn from each other
 - Generates value from our diversity, testing alternate approaches, promoting the best

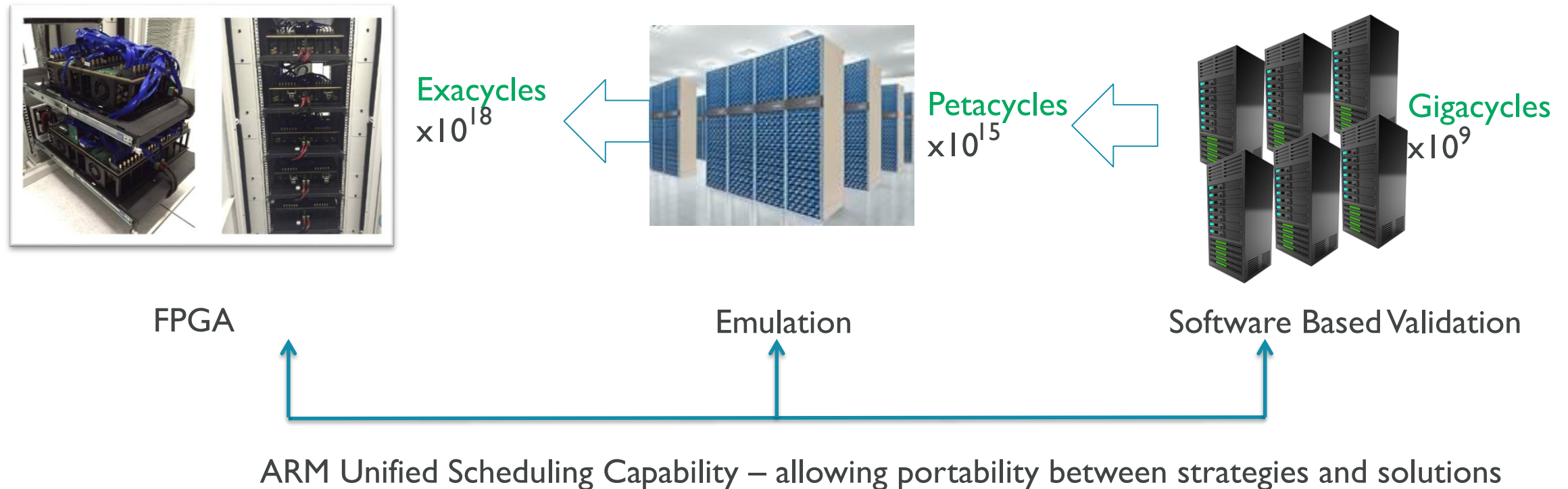


Hardware Verification Flow



Shift left initiative

- ARM has been delivering best-in-class silicon IP for over 25 years
- We fight the demands of increasing complexity, yet delivering more, earlier and earlier
- To meet these demands, ARM developed an internal initiative called “Shift Left”



Accelerating design and validation

- ARM computing subsystems are in everything we rely on today
- Products are becoming more intelligent, more connected, and used in ever more mission and safety critical applications
- ARM has always prided itself on the 'fully verified' nature of its products
- Shift Left is a platform-based initiative to run ever increasing cycles, across a wide range of hardware accelerated platforms (emulation and FPGA), and eliminate bugs from designs EARLIER
- ARM deploys a wide range of solutions for intelligently targeting bugs, and maximising the value of validation payloads
- ARM leverages subsystem validation for all primary market segments
- Subsystems are a key part of the ARM validation strategy allowing real-life scenarios to be validated across thousands of billions of cycles
- These validated subsystems are being ever-opened to our partners

Recent evolution of FPGA-based prototyping in ARM

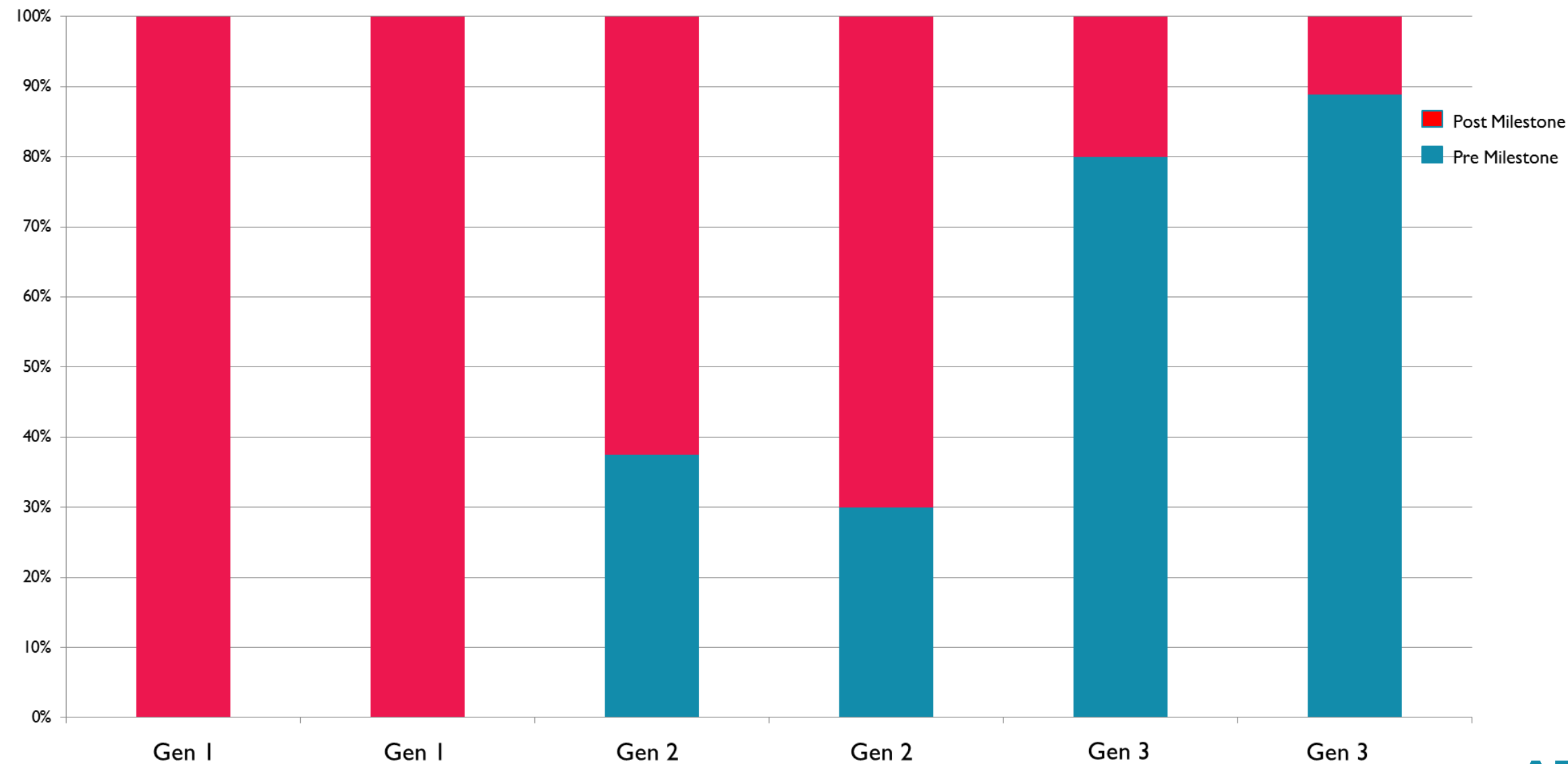
Expanding use into HW verification & HW/SW validation

- Use FPGA-based prototypes for HW verification of ARM IP
 - CPU, Media and System IP products
- Evolved our in-house platforms to support this strategy
 - Single Xilinx V7 Logic Tile
 - 6x Xilinx V7 FPGA board
- Focus on finding defects earlier in the IP development cycle
 - “Shift-Left” strategy for IP verification
- Continue to use FPGA prototypes for SW development and testing
- Moving to commercially-available platforms for future capacity
 - Up-scaling FPGA capacity to a shared **enterprise-class** capability
 - Allows us to run numbers of cycles otherwise achievable only on test silicon

Custom FPGA Prototype Board



Shift Left in action—bugs found on FPGA per generation



Shift left: Increasing use of formal methods

Example CPU: 35% of bugs found by formal with 11% of compute.

Method	Compute%
Simulation	76.37%
Formal	6.65%
Isa-formal	3.96%
Implementation	1.92%
Debug	1.89%
Synthesis	1.39%
Bamboo	0.60%
Other	7.20%
Total	100%

simulation bugs in JIRA	42
Basic formal bugs in JIRA	14
ISA-F bugs in JIRA	9
Total bugs in JIRA	65

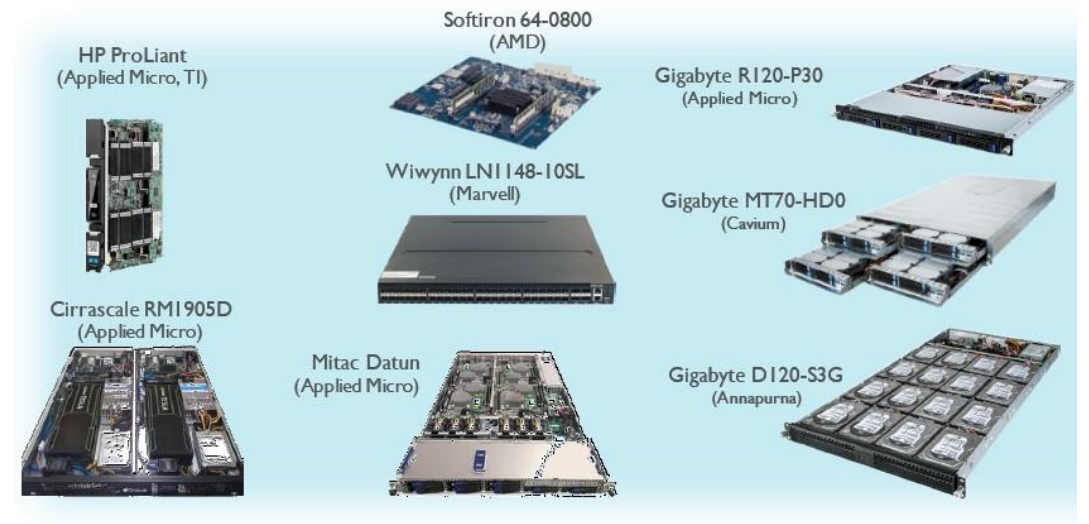
In this example CPU:

- 87% of compute found 64% of bugs with sim
- 7.5% of compute found 22% of bugs with basic formal
- 5% of the compute found 14% of bugs with our isa-formal tool

We are increasing our use of formal methods

ARM powered engineering

- TSG is enabling ARM engineering to adopt ARM as a preferred platform for development
- This is enabled through internal and external partner collaboration
- Initially this will comprise a 5,000 slot deployment
- Later this will be ramped across the organisation and leveraged in the cloud
- TCO savings (\$) using ARM powered compute for engineering purposes are anticipated to be considerable



How ARM helps with your design and verification

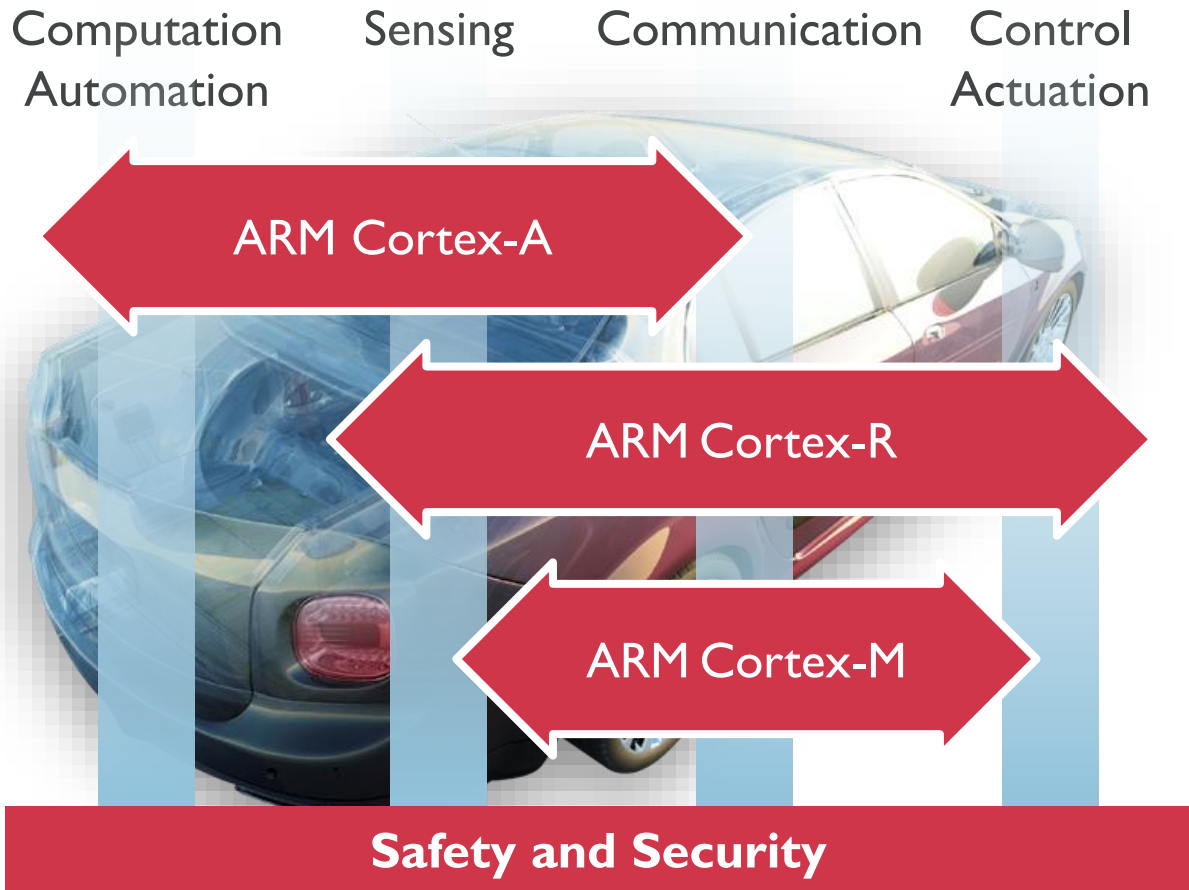
Automotive and functional safety



Validation of mission critical products

Functional safety

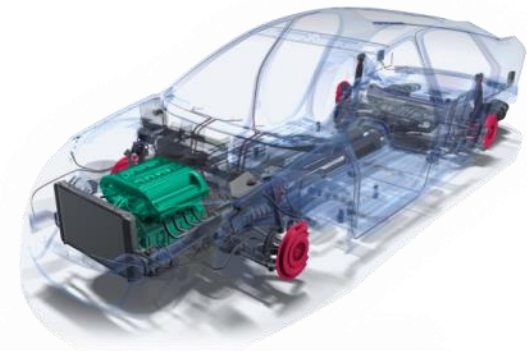
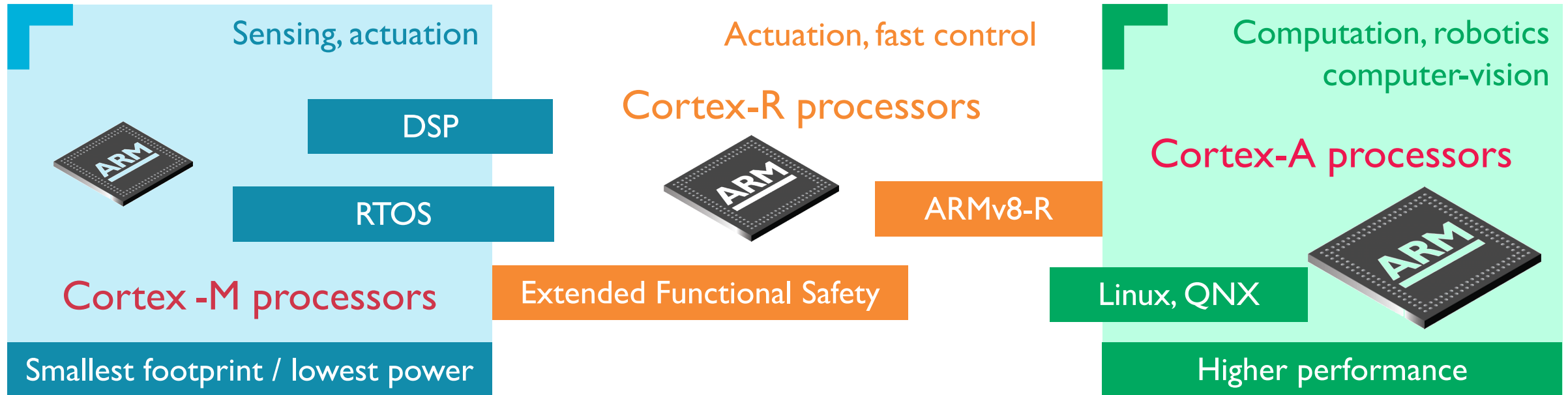
The road ahead – ARM's methodologies evolve to support safety critical demands



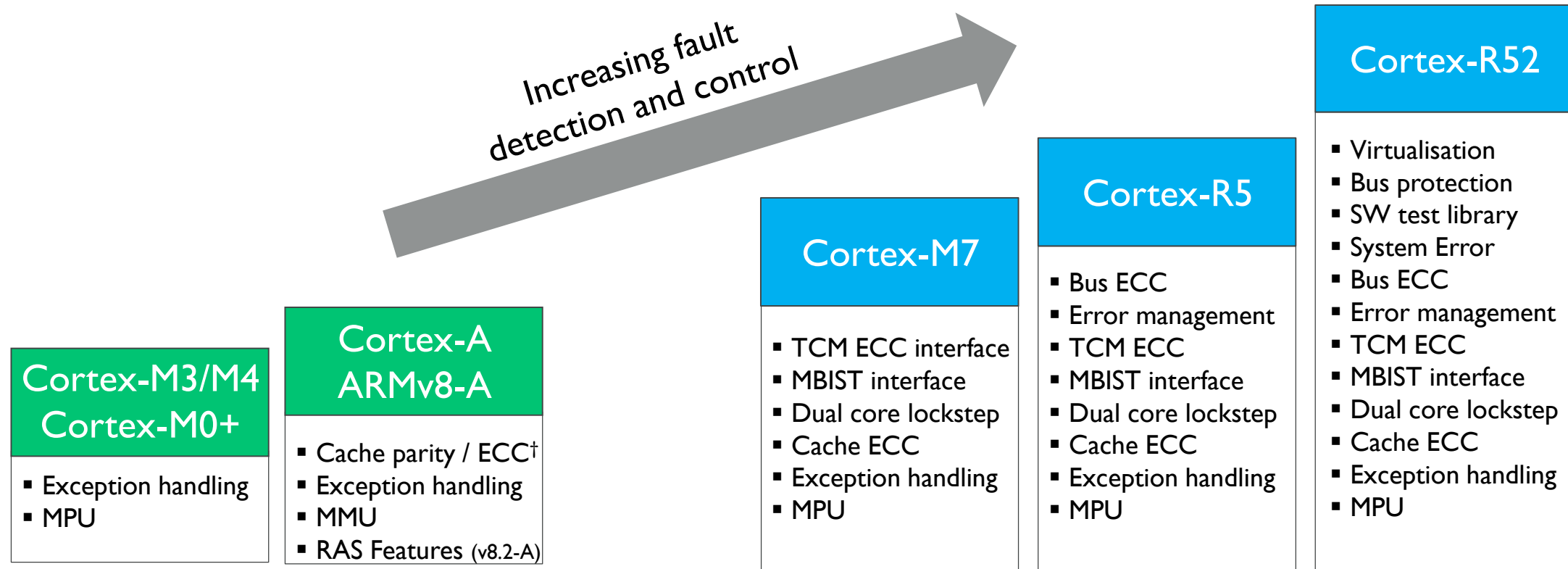
- Driving on the state-of-the-art
 - High performance, low power, safety-related
- Product innovation and integration
 - ARMv8-R real-time virtualization
 - Consolidation of safety-related applications
- Autonomous cars moving ahead
 - Several OEM announcements for 2020
 - Legislative changes in different regions
- Scope of safety is expanding to new areas

Energy-efficient processors for embedded designs

Low power processing is increasingly important for safety applications



Functional safety for ARM Cortex processors



ASIL B systematic capability

- Standard safety package: Safety Manual, FMEA Report, Development Interface Report

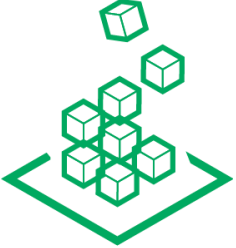
ASIL D systematic capability

- Extended safety package: Safety Manual, FMEA Report, Development Interface Report
- Third party functional safety assessment report

Cortex-R52—most advanced processor for functional safety



Software separation
Hype mode with 2 Level MPU

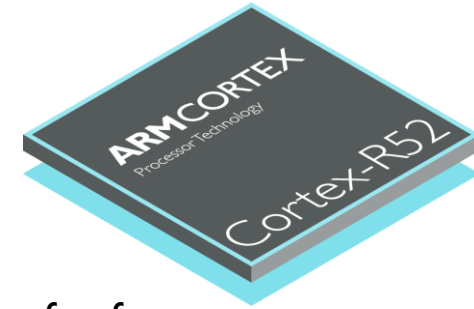


Standard architecture
#1 ecosystem of partners



Functional safety
Safety certified

- Advanced features for Functional Safety
 - ARM's most extensive fault detection and control capabilities
 - Managing both random and systematic faults in processor and memory
 - Comprehensive protection, monitoring and reporting
 - Supporting demanding Industrial SIL 3 or Automotive ASIL D applications
- Address demanding functional safety applications
 - By reducing safety critical software complexity through strong separation of software
 - By offering the most comprehensive set of hardware safety features
 - While maintaining highly deterministic execution of tasks for real time applications
- Combined with key real-time performance enhancements
 - High throughput combined with deterministic responsiveness
 - Multicore capable. Advanced SIMD. Embedded Flash memory interface etc.
 - Meeting ever-increasing performance demands of deeply embedded systems



ARM Compiler 5 support for functional safety

- Compiler Safety Package for software development in safety markets
 - Industrial control, automotive, medical, transportation, military and others

Qualification Kit

- Development process docs
- Safety manual
- Defect report
- Test report



Extended Maintenance

- Five year commitment
- Technical support
- Critical defect fixes



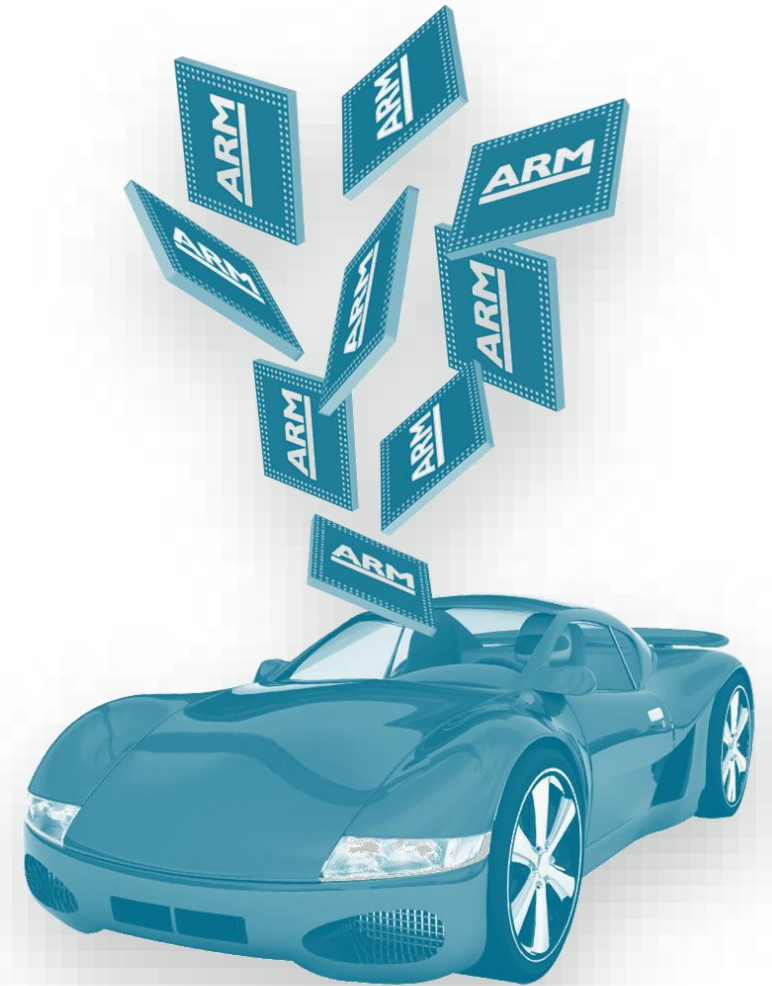
Functional Safety Certified

- TÜV SÜD certification
- ISO 26262 (ASILD)
- IEC 61508 (SIL3)

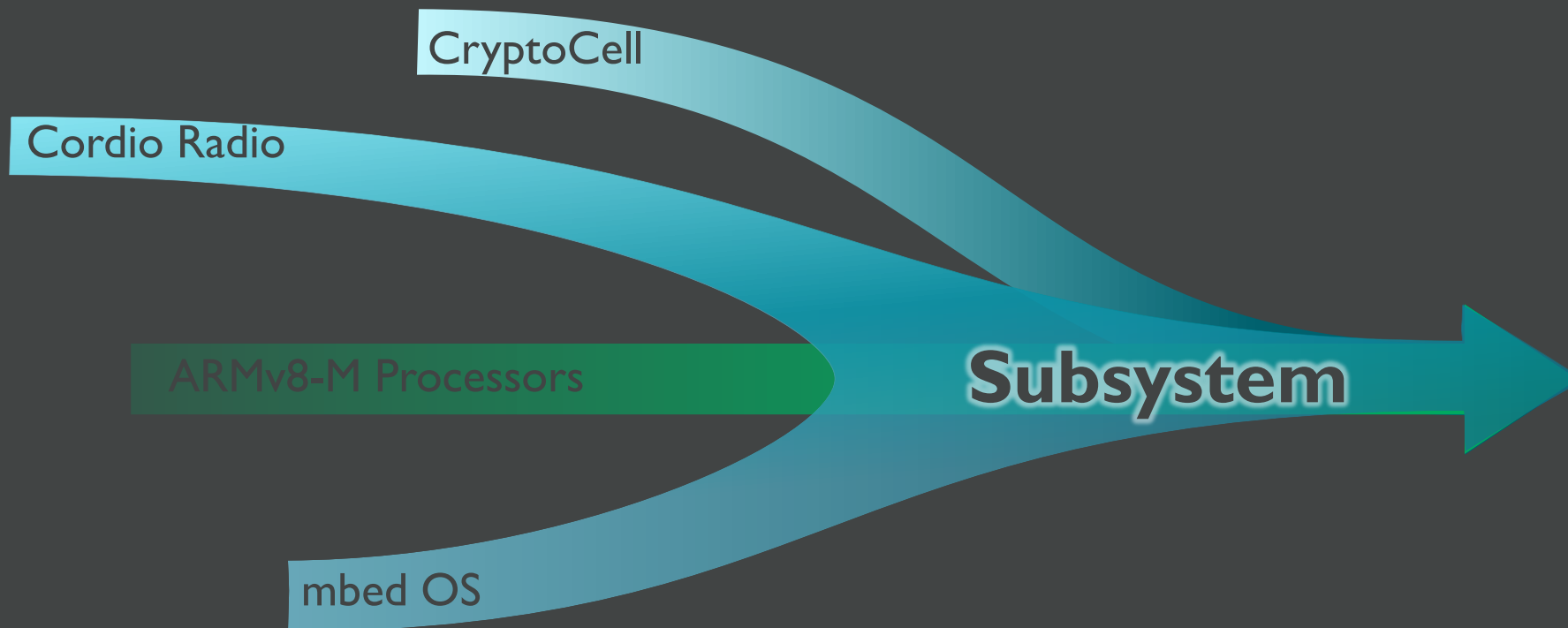


Driving the industry with safety verified solutions

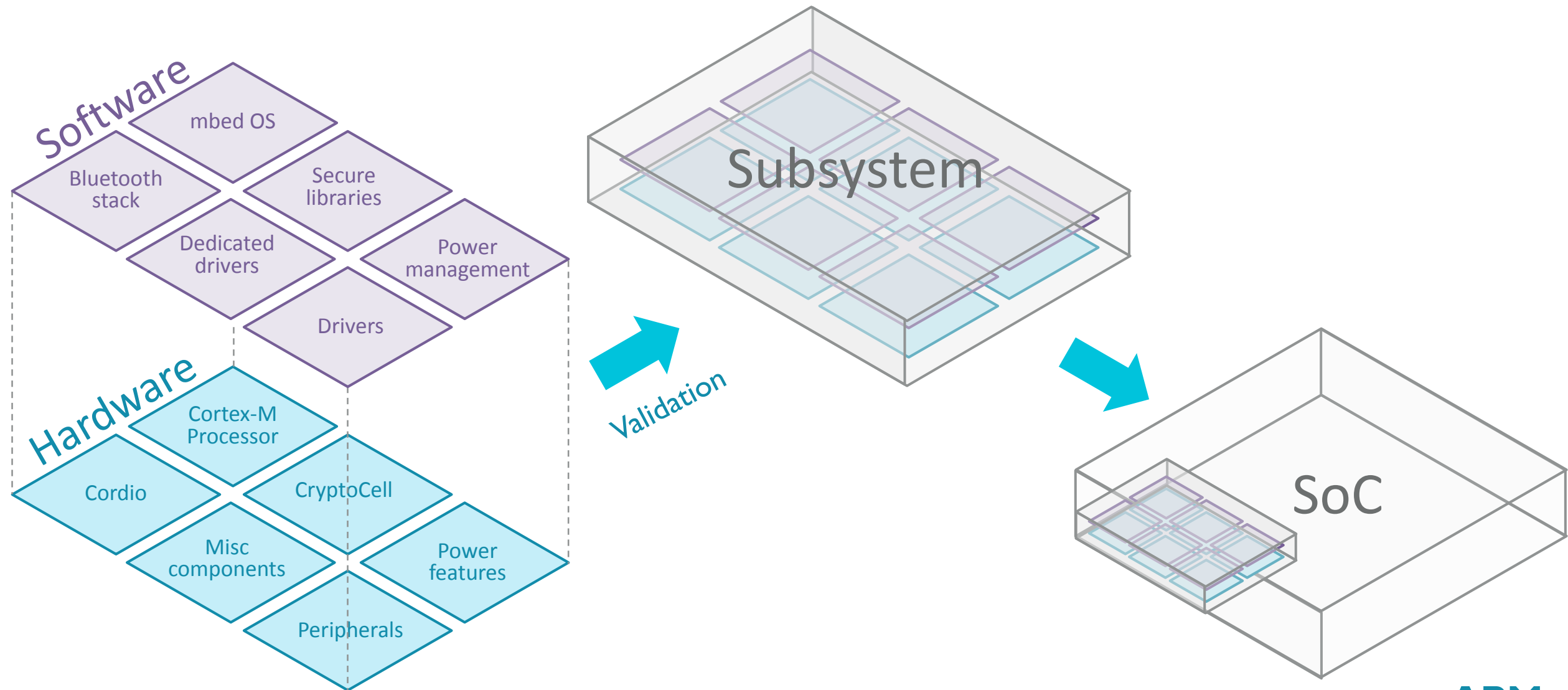
- ARM support for functional safety
 - Safety Manual
 - FMEA Report
 - Development Interface Report
 - SW self-test library for selected products
- Safety support for processors with focus on ARMv8-based products
- Supported by other ARM products and ecosystem partners
 - Compilers with qualification and certification information
 - Analysis tools



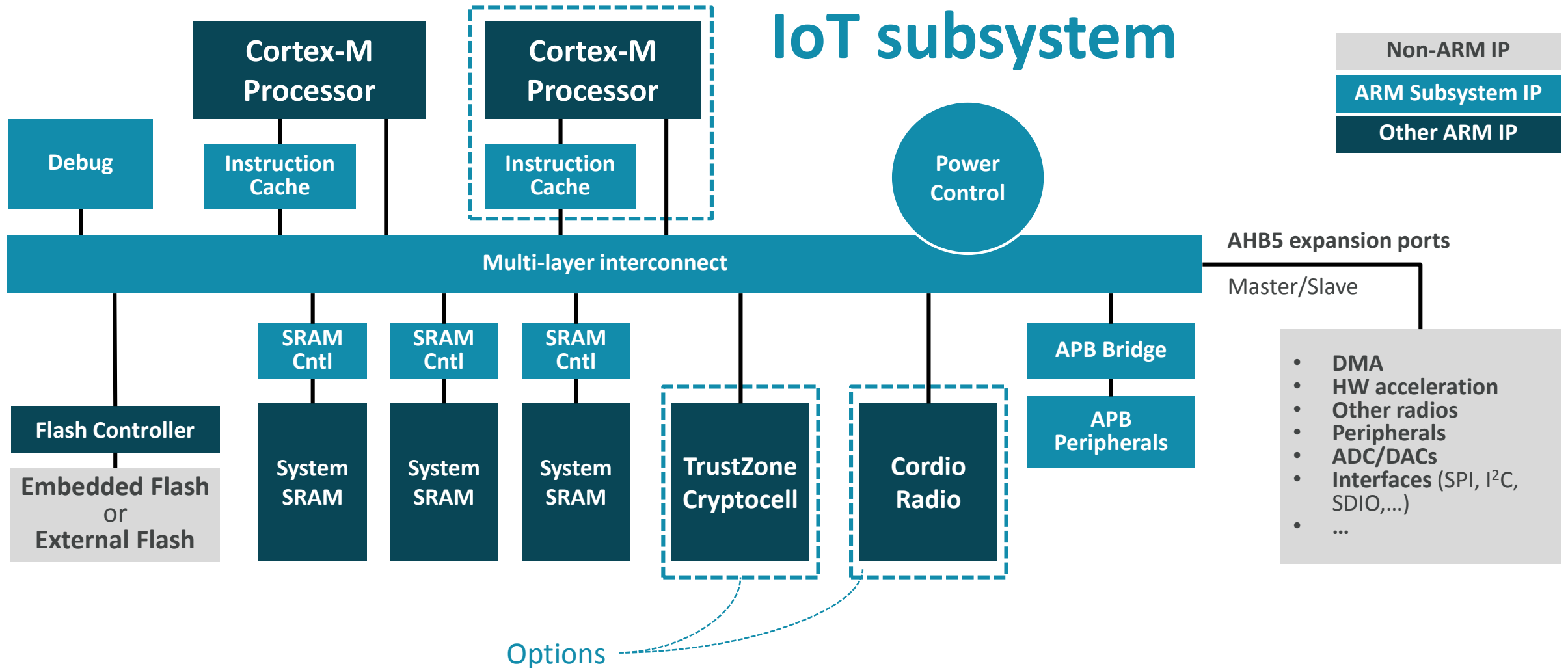
IoT subsystem example – accelerating time to market



What is an IoT subsystem?



IoT subsystem hardware

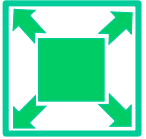


ARM Cordio radio IP—sub 1 volt, lowest power radio solution



Flexible

Enables innovation, differentiation and faster time to market



Complete

A complete Bluetooth low energy and 802.15.4 connectivity solution IP
'RF to Application' – Bluetooth Qualified



Efficient

120% more battery life than best-in-class, Bluetooth low energy solutions



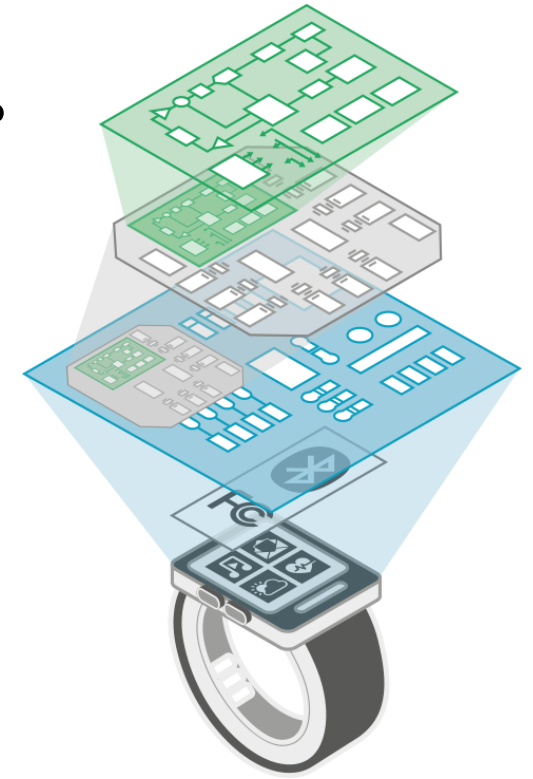
**Smallest total
Footprint**

Enables smaller, cheaper and more reliable devices
Low gate count, **Only 11** external BOM components



Fast

Fast time to new standards, fast time to market
Short development time, lower development costs



Example FPGA prototyping for partners—Cortex-M

- Designed for evaluation and prototyping
 - IoT subsystem on FPGA
 - Daughter board with radio
 - **mbed pre-ported**, ready to extend with differentiating IP
- **Rapid** software and hardware development
 - Ready for software development
 - Code porting, debugging and profiling
 - Ready for hardware integration with differentiating IP
- Expandable
 - Large FPGA for user logic
 - Arduino shield adapter
 - I/O expansion and multiple debug connectors for tool vendors



Major benefits to design and verification using subsystems

- Saves **time**

- Design with a pre-assembled system
- Ready to extend with differentiating peripherals

- Accelerates **time to market**

- Pre-verified
- Pre-qualified radio

- Reduces **risk**

- Verified and tested on FPGA
- Radio is silicon-proven
- Security is built-in

- Saves **effort**

- System optimized for mbed and other RTOS
- System architecture designed for IoT
- The subsystem provides the base, partners concentrate on value-adding features

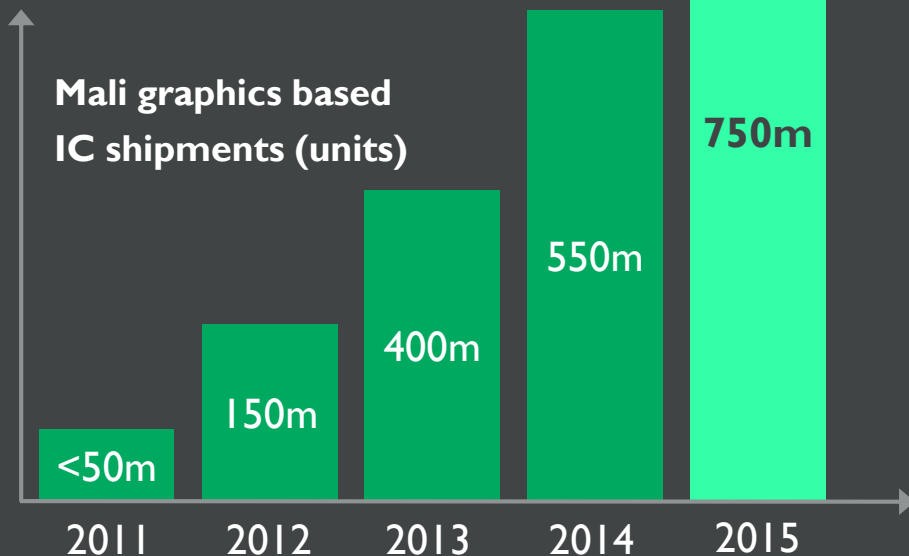
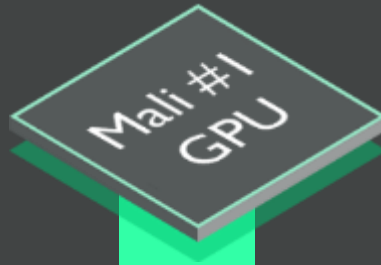
- **Extensible** platform

- Ready to plug other peripherals
- Accepts other radios
- System easy to prototype

It doesn't stop with CPU...

750M

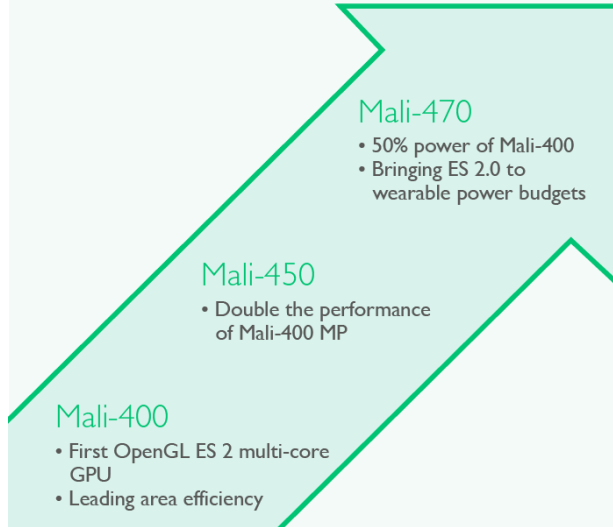
Mali-based
GPUs shipped
in 2015



GPU, Video, Display,
Intelligent Visual Products
Driving more intelligence into media processing

Solutions for all types of devices

Ultra-Low Power

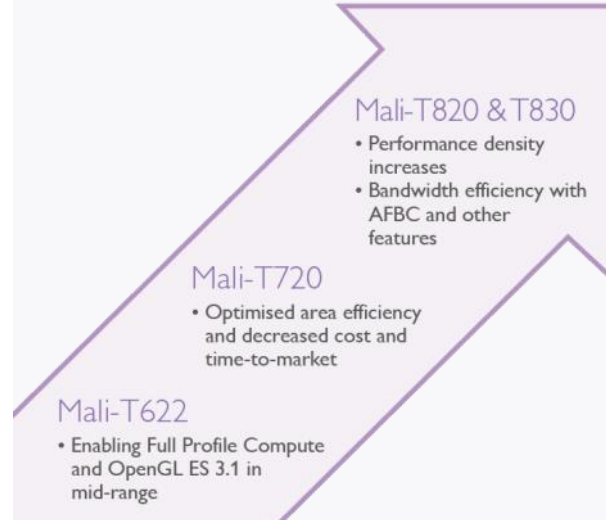


Smart watch



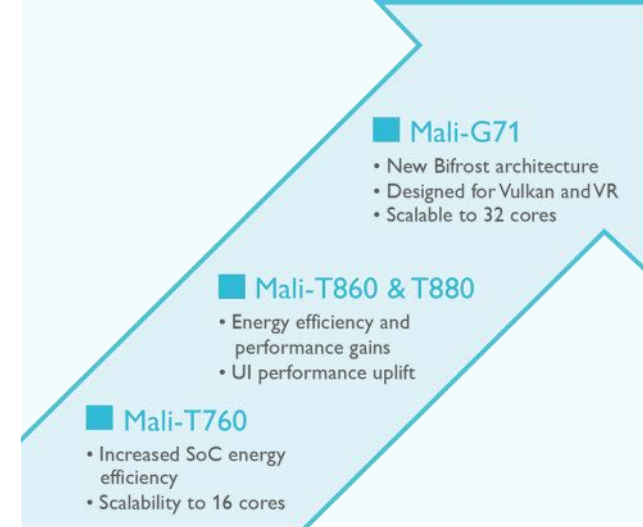
Smart TV

High Area Efficiency



Clamshell device

High Performance



Premium phone

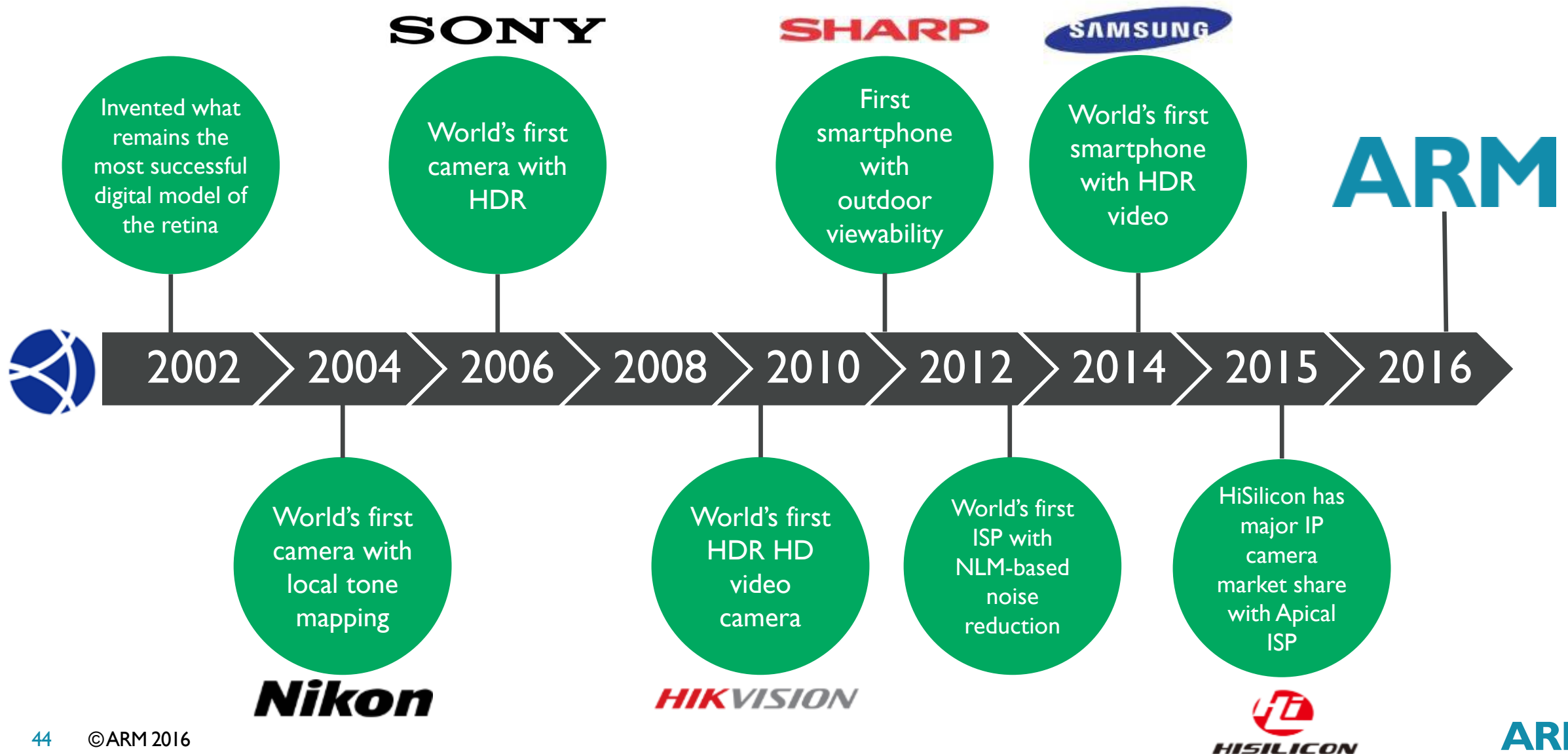


Virtual reality

New use cases will continue driving demands

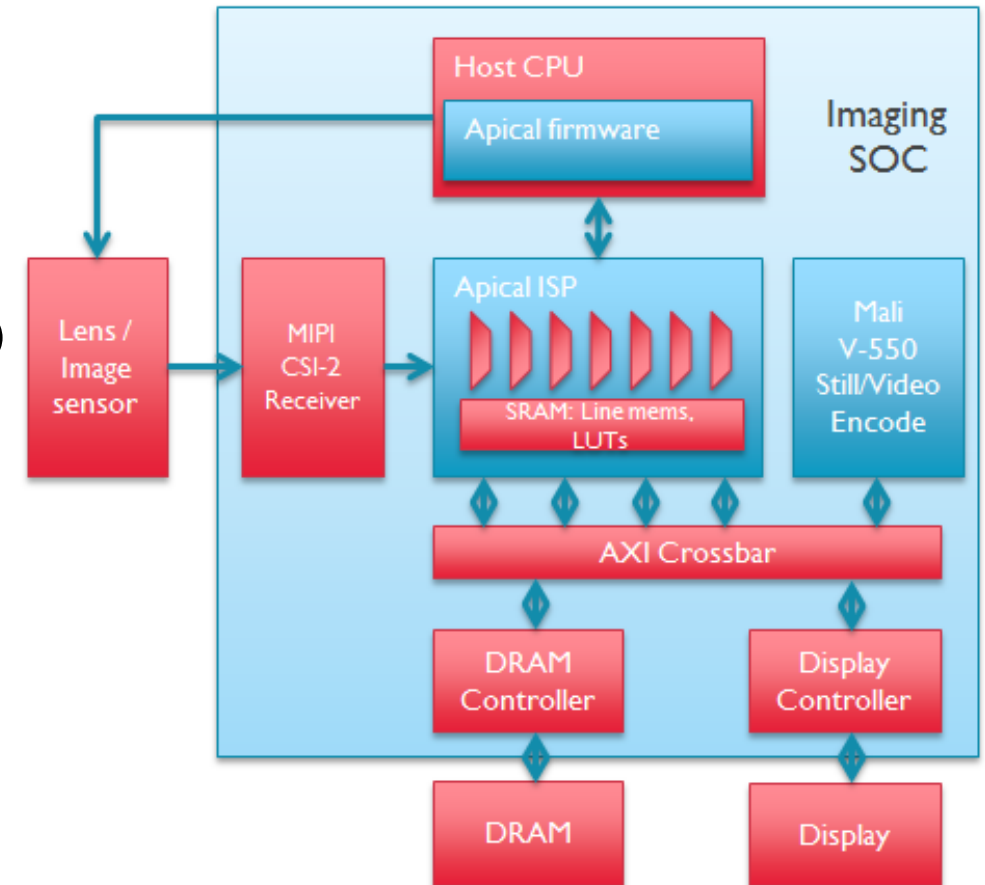


Use cases underpinned by image processing: ARM with Apical



Camera – image signal processor

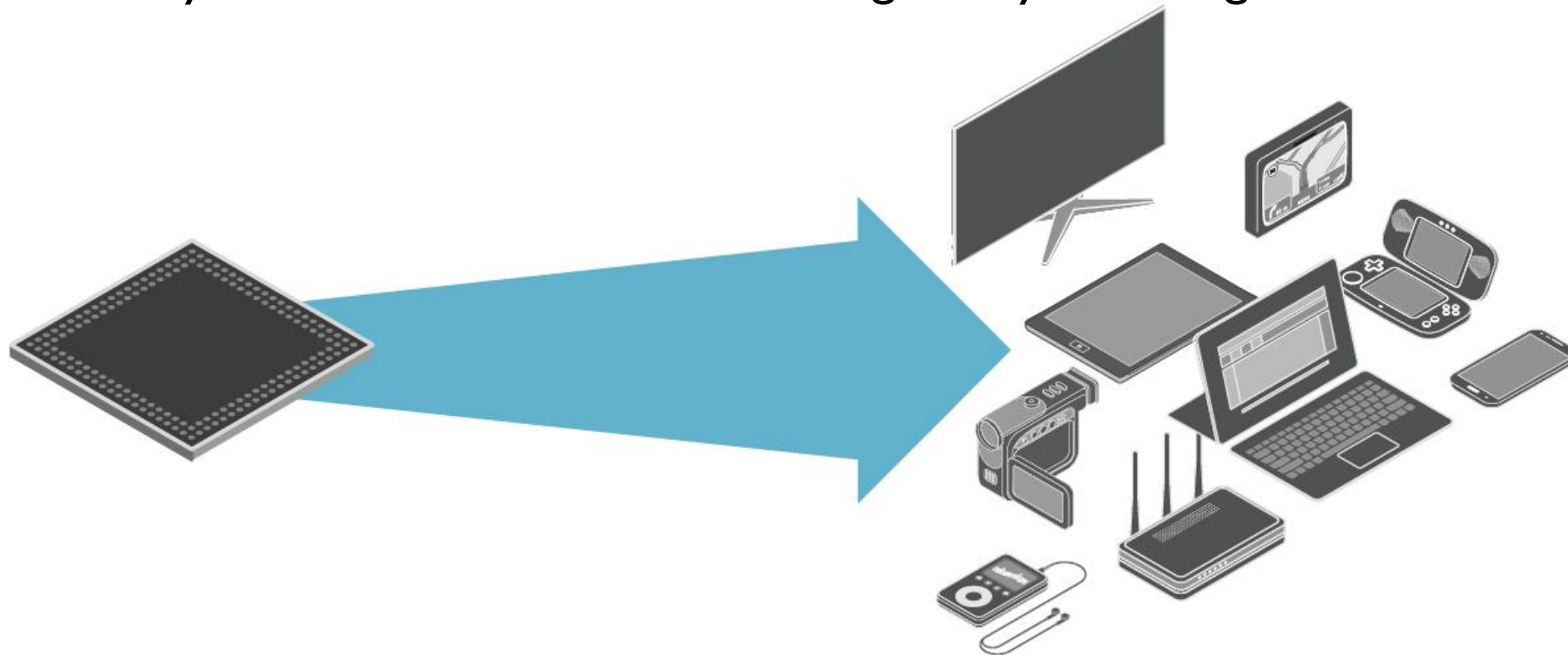
- Features
 - Lens shading (vignetting) correction (mesh and radial) and Geometric Distortion Correction engine
 - Advanced spatial (2D) noise reduction (sinter[®])
 - Motion-adaptive temporal (3D) noise reduction (temper[™])
 - Multi-exposure HDR image fusion
 - Space-variant HDR processing (iridix[®])
- Performance
 - >500Mpixel/sec
 - 1080p60/4K video
 - 256Mpixel sensor support
- Deliverables
 - Hardware IP, firmware, tuning software and support



Where innovation begins

We have spoken ARM's D&V, and how we can help your D&V

- ARM continues to innovate and bring new, exciting products to market
- TSG continually rises to meet ARM's own growing D&V requirements
- Our partners will continue to benefit from ARM and TSG innovation
- Thank you – we look forward to talking with you during the show





ARM

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